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GENNUM

GS9090 GenLINX® III 270Mb/s Deserializer for SDI and DVB-ASI

GS9090 Data Sheet

Key Features

- SMPTE 259M-C compliant descrambling and NRZI to NRZ decoding (with bypass)
- DVB-ASI sync word detection and 8b/10b decoding
- Integrated line-based FIFO for data alignment/delay, clock phase interchange, DVB-ASI data packet extraction and clock rate interchange, and ancillary data packet extraction
- Integrated VCO and reclocker
- Automatic or manual selection between SMPTE video and DVB-ASI data
- Single serial digital input buffer with wide input sensitivity
- User selectable additional processing features including:
  - TRS, ANC data checksum, and EDH CRC error detection and correction
  - programmable ANC data detection
  - illegal code remapping
- Internal flywheel for noise immune H, V, F extraction
- Automatic standards detection and indication
- Enhanced Gennum Serial Peripheral Interface (GSPI)
- JTAG test interface
- Polarity insensitive for DVB-ASI and SMPTE signals
- +1.8V core power supply with optional +1.8V or +3.3V I/O power supply
- Small footprint (8mm x 8mm)
- Low power operation (typically 145mW)
- Pb-free and RoHS compliant

Applications

- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS9090 is a 270Mb/s reclocking deserializer with an internal FIFO. When used in conjunction with one of Gennum's SDI Cable Equalizers, a receive solution for SD-SDI and DVB-ASI applications can be realized.

In addition to reclocking and deserializing the input data stream, the GS9090 performs NRZI-to-NRZ decoding, descrambling as per SMPTE 259M-C, and word alignment when operating in SMPTE mode. When operating in DVB-ASI mode, the device will word align the data to K28.5 sync characters and 8b/10b decode the received stream.

The integrated reclocker features a very wide Input Jitter Tolerance, and is fully compatible with both SMPTE and DVB-ASI input streams.

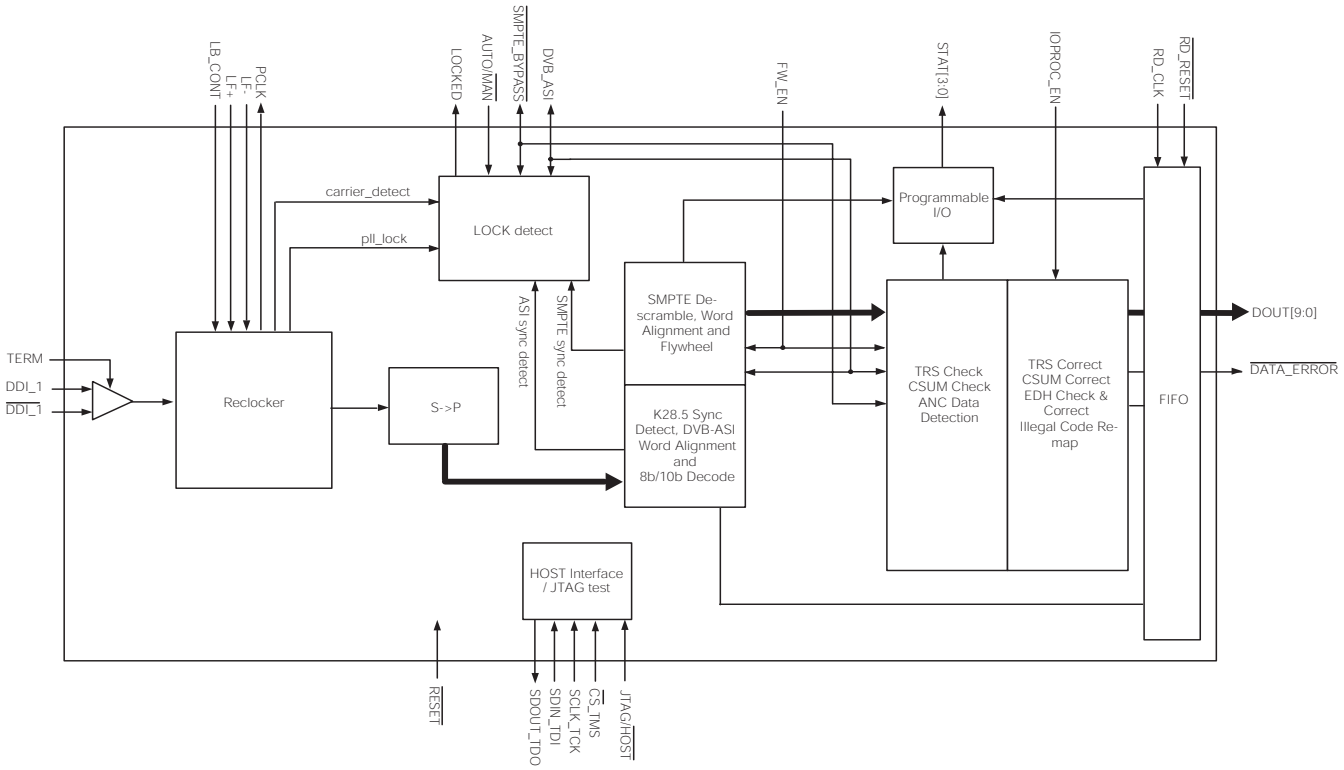
The GS9090 includes a range of data processing functions such as error detection and correction, automatic standards detection, and EDH support. The device can also detect and extract SMPTE 352M payload identifier packets and independently identify the received video standard. This information is read from internal registers via the host interface port.

TRS errors, EDH CRC errors, and ancillary data checksum errors can all be detected and corrected. A single $\overline{\text{DATA\_ERROR}}$ pin is provided which is an inverted logical 'OR'ing of all detectable errors. Individual error status is stored in internal 'ERROR_STATUS' registers.

The GS9090 also incorporates a video line-based FIFO. This FIFO may be used in four user-selectable modes to carry out tasks such as data alignment / delay, clock phase interchange, MPEG packet extraction and clock rate interchange, and ancillary data packet extraction.

Parallel data outputs are provided in 10-bit multiplexed format, with the associated parallel clock output signal operating at 27MHz.

The GS9090 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS compliant).



GS9090 Functional Block Diagram

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1. Pin Out

1.1 Pin Assignment

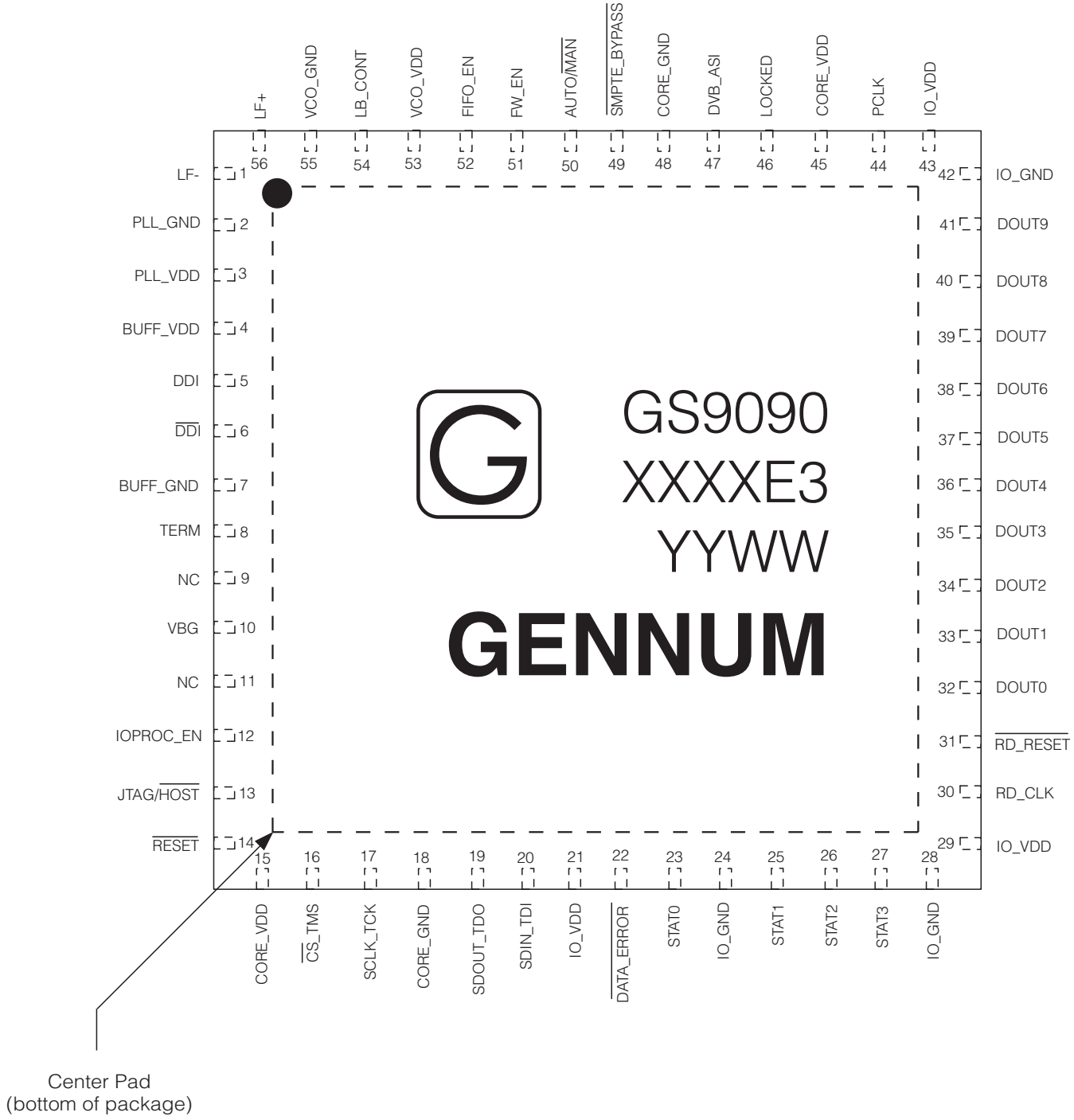

Figure 1-1: Pin Assignment

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	LF-	Analog	Input	Loop filter component connection. Connect to pin 56 (LF+) as shown in the Typical Application Circuit (Part B) on page 67.
2	PLL_GND	Analog	Input Power	Ground connection for phase-locked loop. Connect to GND.
3	PLL_VDD	Analog	Input Power	Power supply connection for phase-locked loop. Connect to +1.8V DC.
4	BUFF_VDD	Analog	Input Power	Power supply connection for digital input buffers. When operating with 1.8V input as required by the current silicon this pin should be left unconnected. When operating with 3.3V input (available in future silicon) this pin should be connected to +3.3V as shown in the Typical Application Circuit (Part B) on page 67.
5, 6	DDI, $\overline{\text{DDI}}$	Analog	Input	Serial digital differential input pair.
7	BUFF_GND	Analog	Input Power	Ground connection for serial digital input buffer. Connect to GND.
8	TERM	Analog	Input	Termination for serial digital input. AC couple to BUFF_GND
9, 11	NC	–	–	No connect.
10	VBG	Analog	Input	Bandgap filter capacitor. Connect to GND as shown in the Typical Application Circuit (Part B) on page 67.
12	IOPROC_EN	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal Levels are LVCMOS / LVTTL compatible. Used to enable or disable the I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • Illegal Code Remapping • EDH CRC Error Correction • Ancillary Data Checksum Error Correction • TRS Error Correction • EDH Flag Detection To enable a subset of these features, keep the IOPROC_EN pin HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When set LOW, the device will enter low-latency mode. NOTE: When the internal FIFO is configured for Video mode or Ancillary Data Extraction mode, the IOPROC_EN pin must be set HIGH (see Internal FIFO Operation on page 46).

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
13	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation.
14	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to reset the internal operating conditions to default setting or to reset the JTAG test sequence. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): When asserted LOW, all functional blocks will be set to default conditions and all output signals become high impedance with the exception of the STAT pins and the $\overline{\text{DATA\_ERROR}}$ pin which will maintain the last state they were in for the duration that $\overline{\text{RESET}}$ is asserted. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes. NOTE: See Device Power Up on page 64 for power on reset requirements.
15, 45	CORE_VDD	Non Synchronous	Input Power	Power supply for digital logic blocks. Connect to +1.8V DC. NOTE: For power sequencing requirements, see Device Power Up on page 64.
16	$\overline{\text{CS}}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Chip Select / Test Mode Select Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): $\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): $\overline{\text{CS}}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH.
17	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Clock / Test Clock. All JTAG / Host Interface address and data are shifted into/out of the device synchronously with this clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SCLK_TCK operates as the host interface serial data clock, SCLK. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SCLK_TCK operates as the JTAG test clock, TCK.
18, 48	CORE_GND	Non Synchronous	Input Power	Ground connection for digital logic blocks. Connect to GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
19	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SDOUT_TDO operates as the JTAG test data output, TDO.
20	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Input / Test Data Input Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): SDIN_TDI operates as the JTAG test data input, TDI.
21, 29, 43	IO_VDD	Non Synchronous	Input Power	Power supply for digital I/O. For a 3.3V tolerant I/O, connect pins to either +1.8V DC or +3.3V DC. For a 5V tolerant I/O, connect pins to a +3.3V DC. NOTE: For power sequencing requirements, see Device Power Up on page 64.
22	$\overline{\text{DATA\_ERROR}}$	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. The $\overline{\text{DATA\_ERROR}}$ signal will be LOW when an error within the received data stream has been detected by the device. This pin is an inverted logical 'OR'ing of all detectable errors listed in the internal ERROR_STATUS register. Once an error is detected, $\overline{\text{DATA\_ERROR}}$ will remain LOW until the start of the next video frame / field, or until the ERROR_STATUS register is read via the host interface. The $\overline{\text{DATA\_ERROR}}$ signal will be HIGH when the received data stream has been detected without error. NOTE: It is possible to program which error conditions are monitored by the device by setting appropriate bits in the ERROR_MASK register HIGH. All error conditions are detected by default.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
23, 25, 26, 27	STAT[0:3]	Synchronous with PCLK or RD_CLK	Output	MULTI FUNCTION I/O PORT Signal levels are LVCMOS / LVTTL compatible. Programmable multi-function outputs. By programming the bits is the IO_CONFIG register, each pin can output one of the following signals: • H • V • F • $\overline{\text{FIFO\_LD}}$ • ANC_DETECT • EDH_DETECT • FIFO_FULL • FIFO_EMPTY These pins are set to certain default values depending on the configuration of the device and the internal FIFO mode selected. See Programmable Multi-Function Outputs on page 56 for details.
24, 28, 42	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O. Connect to GND.
30	RD_CLK	–	Input	FIFO READ CLOCK Signal levels are LVCMOS / LVTTL compatible. The application layer clocks the parallel data out of the FIFO on the rising edge of RD_CLK.
31	$\overline{\text{RD\_RESET}}$	Synchronous with RD_CLK	Input	FIFO READ RESET Signal levels are LVCMOS / LVTTL compatible. Valid input only when the device is in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH and DVB-ASI = LOW), and the internal FIFO is configured for video mode (see Video Mode on page 46). A HIGH to LOW transition will reset the FIFO pointer to address zero of the memory.
32 - 41	DOUT[0:9]	Synchronous with RD_CLK or PCLK	Output	PARALLEL VIDEO DATA BUS Signal levels are LVCMOS / LVTTL compatible. When the internal FIFO is enabled and configured for either video mode or DVB-ASI mode, parallel data will be clocked out of the device on the rising edge of RD_CLK. When the internal FIFO is in bypass mode, parallel data will be clocked out of the device on the rising edge of PCLK. DOUT9 is the MSB and DOUT0 is the LSB.
44	PCLK	–	Output	PIXEL CLOCK OUTPUT Signal levels are LVCMOS / LVTTL compatible. 27MHz parallel clock output.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
46	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. The LOCKED signal will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode, or when the reclocker has achieved lock in Data-Through mode. It will be LOW otherwise. When the signal is LOW, all digital output signals will be forced to logic LOW levels.
47	DVB_ASI	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This pin is an input set by the application layer in Manual mode, and an output set by the device in Auto mode. Auto Mode (AUTO/$\overline{\text{MAN}}$ = HIGH): The DVB_ASI signal will be HIGH only when the device has locked to a DVB-ASI compliant data stream. It will be LOW otherwise. Manual Mode (AUTO/$\overline{\text{MAN}}$ = LOW): When the application layer sets this pin HIGH, the device will be configured to operate in DVB-ASI mode. The $\overline{\text{SMPTE\_BYPASS}}$ pin will be ignored. When set LOW, the device will not support the decoding or word alignment of received DVB-ASI data.
49	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input / Output	CONTROL SIGNAL INPUT / STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This pin is an input set by the application layer in Manual mode, and an output set by the device in Auto mode. Auto Mode (AUTO/$\overline{\text{MAN}}$ = HIGH): The $\overline{\text{SMPTE\_BYPASS}}$ signal will be HIGH only when the device has locked to a SMPTE compliant data stream. It will be LOW otherwise. When the signal is LOW, no I/O processing features are available. Manual Mode (AUTO/$\overline{\text{MAN}}$ = LOW): When the application layer sets this pin HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When the $\overline{\text{SMPTE\_BYPASS}}$ pin is set LOW, the device will not support the descrambling, decoding, or word alignment of received SMPTE data. No I/O processing features will be available.
50	AUTO/$\overline{\text{MAN}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. When set HIGH, the GS9090 will operate in Auto mode. The DVB_ASI and $\overline{\text{SMPTE\_BYPASS}}$ pins become output status signals set by the device. In this mode, the GS9090 will automatically detect, reclock, deserialize, and process SMPTE or DVB-ASI compliant input data. When set LOW, the GS9090 will operate in Manual mode. The DVB_ASI and $\overline{\text{SMPTE\_BYPASS}}$ pins become input control signals. In this mode, the application layer must set these two external pins for the correct reception of either SMPTE or DVB-ASI data. Manual mode also supports the reclocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
51	FW_EN	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable the noise immune flywheel of the device. When set HIGH, the internal flywheel is enabled. This flywheel is used in the extraction of timing signals, the generation of TRS signals, the automatic detection of video standards, and in manual switch line lock handling. When set LOW, the internal flywheel is disabled. Timing based TRS errors will not be detected.
52	FIFO_EN	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable / disable the internal FIFO. When FIFO_EN is HIGH, the internal FIFO will be enabled. Data will be clocked out of the device on the rising edge of the RD_CLK input pin if the FIFO is in video mode or DVB-ASI mode. When FIFO_EN is LOW, the internal FIFO is bypassed and parallel data is clocked out on the rising edge of the PCLK output.
53	VCO_VDD	Analog	Input Power	Power supply connection for Voltage-Controlled-Oscillator. Connect to +1.8V DC.
54	LB_CONT	Analog	Input	CONTROL SIGNAL INPUT Control voltage to fine-tune the loop bandwidth of the PLL.
55	VCO_GND	Analog	Input Power	Ground connection for Voltage-Controlled-Oscillator. Connect to GND.
56	LF+	Analog	Input	Loop filter component connection. Connect to pin 1 (LF-) as shown in the Typical Application Circuit (Part B) on page 67.
–	Center Pad	–	Power	Connect to GND following the Recommended PCB Footprint on page 69

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +3.47V
Input Voltage Range (any input)	-2.0V to + 5.25V
Ambient Operating Temperature	$-20°C \leq T_A \leq 85°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
ESD protection on all pins (see note 2)	1kV

NOTES:
1. See reflow solder profile
2. HBM, per JESDA - 114B

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Operating Temperature Range	T_A	–	0	25	70	°C	1
Core power supply voltage	CORE_VDD	–	1.71	1.8	1.89	V	–
Digital I/O Buffer Power Supply Voltage	IO_VDD	1.8V Operation	1.71	1.8	1.89	V	–
	IO_VDD	3.3V Operation	3.13	3.3	3.47	V	–
PLL Power Supply Voltage	PLL_VDD	–	1.71	1.8	1.89	V	–
VCO Power Supply Voltage	VCO_VDD	–	1.71	1.8	1.89	V	–
Typical System Power	P_D	CORE_VDD = 1.8V IO_VDD = 1.8V T = 25°C	–	145	–	mW	–
Max. System Power	P_D	CORE_VDD = 1.89V IO_VDD = 3.47V T = 70°C	–	–	200	mW	–

Table 2-2: DC Electrical Characteristics (Continued)

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Digital I/O							
Input Voltage, Logic LOW	V_{IL}	1.8V Operation or 3.3V Operation	–	–	0.35 x IO_VDD	V	–
Input Voltage, Logic HIGH	V_{IH}	1.8V Operation or 3.3V Operation	0.65 x IO_VDD	–	–	V	–
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 8mA @ 3.3V, 4mA @ 1.8V	–	–	0.4	V	–
Output Voltage, Logic HIGH	V_{OH}	I_{OL} = -8mA @ 3.3V, -4mA @ 1.8V	IO_VDD - 0.4	–	–	V	–
Serial Digital Input							
Input Termination Resistance	R_{IN}	–	37.5	50	62.5	Ω	–

NOTES:

1. All DC and AC electrical parameters within specification.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Asynchronous Lock Time (LOCKED signal set HIGH)	t_{LOCK}	Input jitter of 0.2UI, No data to SMPTE, SMPTE_BYPASS = HIGH DVB_ASI = LOW, at 25°C	–	–	235	us	1
Asynchronous Lock Time (LOCKED signal set HIGH)	t_{LOCK}	Input jitter of 0.2UI, No data to DVB-ASI, SMPTE_BYPASS = HIGH DVB_ASI = HIGH, at 25°C	–	–	185	us	1
Asynchronous Lock Time (LOCKED signal set HIGH)	t_{LOCK}	Input jitter of 0.2UI, No data to non-SMPTE, SMPTE_BYPASS = LOW DVB_ASI = LOW, at 25°C	–	–	165	us	1

Table 2-3: AC Electrical Characteristics (Continued)

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Serial Digital Input							
Serial Input Data Rate	DR_{SDI}	–	–	270	–	Mb/s	–
Serial Input Jitter Tolerance	IJT	–	–	0.4	–	UI	2
Serial Digital Input Signal Swing	ΔV_{DDI}	Differential with internal 100Ω input termination	400	800	1700	mV_{p-p}	3
Parallel Output							
Parallel Output Clock Frequency	f_{PCLK}	–	–	27	–	MHz	–
Parallel Output Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Variation of Parallel Output Clock (from 27MHz)	–	Device Unlocked T_A = -20°C to +85°C IO_VDD = 1.8V	-7.5	–	+7.5	%	4
Output Data Hold Time	t_{OH}	With 15pF load	3.0	–	–	ns	5
Output Delay Time	t_{OD}	With 15pF load	–	–	10.0	ns	5
GSPI							
GSPI Input Clock Frequency	f_{GSPI}	–	–	–	54.0	MHz	–
GSPI Clock Duty Cycle	DC_{GSPI}	–	40	–	60	%	–
GSPI Setup Time	t_{GS}	–	1.5	–	–	ns	–
GSPI Hold Time	t_{GH}	–	–	–	1.5	ns	–

NOTES:

1. No signal to signal present, or a switch from another data rate to 270Mb/s.
2. Power supply noise 50mV_{pp} at 15kHz, 100kHz, 1MHz sinusoidal modulation.
3. See Figure 2-1.
4. When the serial input to the GS9090 is removed, the PCLK output signal will continue to operate at 27MHz and the internal VCO will remain at this frequency within +/- 7.5% over the range -20°C to +85°C.
5. Timing includes the following outputs: DOUT[9:0], STAT[3:0]. When the FIFO is enabled, the outputs are measured with respect to RD_CLK.

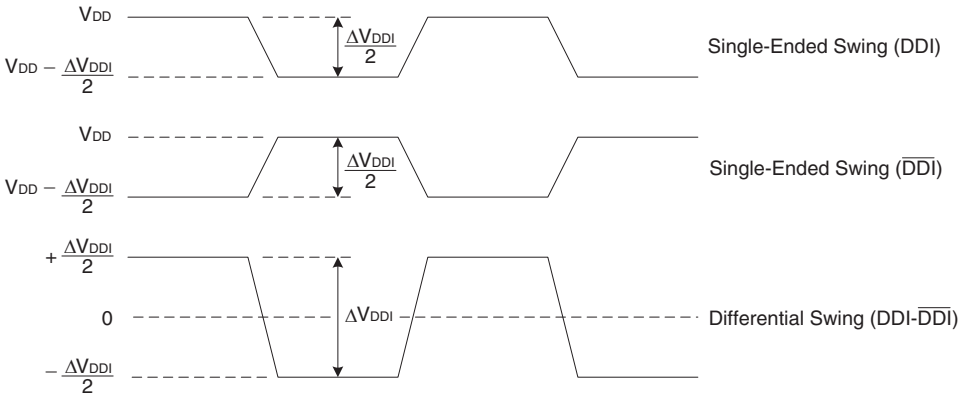

Figure 2-1: Serial Digital Input Signal Swing

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-2. The recommended standard eutectic reflow profile is shown in Figure 2-3.

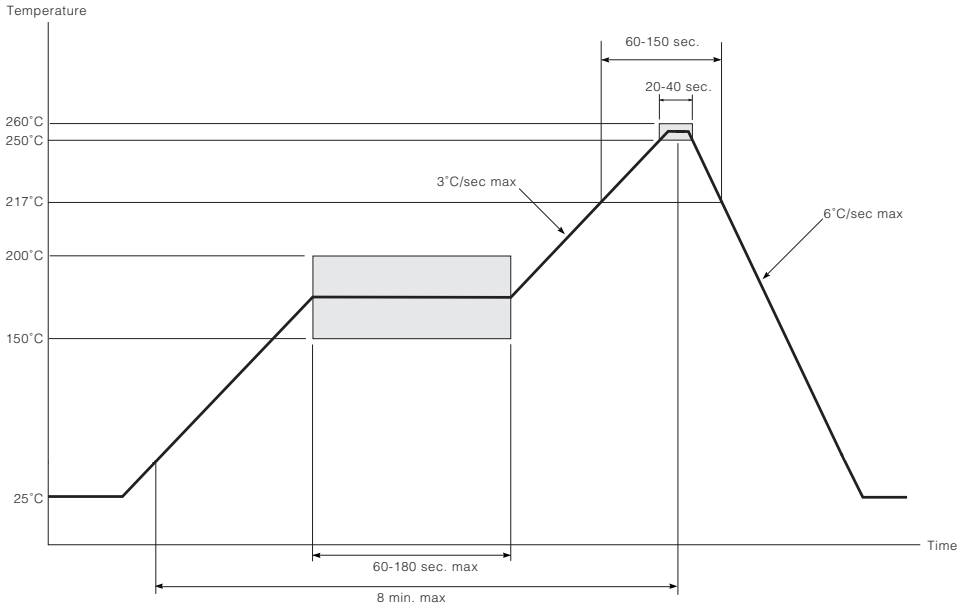

Figure 2-2: Maximum Pb-free Solder Reflow Profile (Preferred)

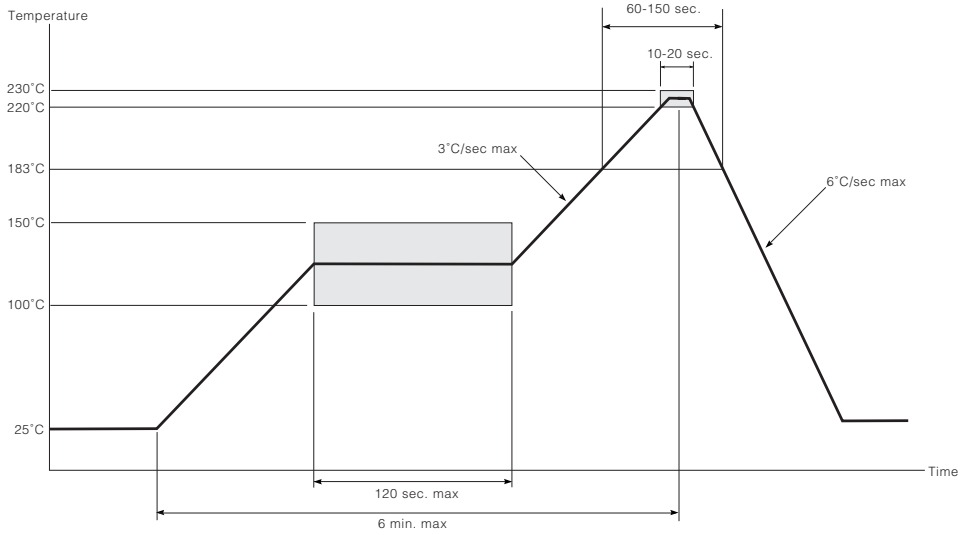

Figure 2-3: Standard Eutectic Solder Reflow Profile (Pb-free package)

2.5 Host Interface Map

Table 2-4: Host Interface Map

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_LD_POSITION[12:0]	28h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	27h																
	26h																
ERROR_MASK_REGISTER	25h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ERR_MASK	FF_CRC_ERR_MASK	AP_CRC_ERR_MASK	LOCK_ERR_MASK	CCS_ERR_MASK	SAV_ERR_MASK	EAV_ERR_MASK
FF_PIXEL_END_F1[12:0]	24h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4[10:0]	14h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B(4,3)	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A(2,1)	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
ANC_TYPE(5)[15:0]	0Eh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(4)[15:0]	0Dh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(3)[15:0]	0Ch	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(2)[15:0]	0Bh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(1)[15:0]	0Ah	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_B[10:0]	09h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_EMPTY_OFFSET	06h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h	Not Used	Not Used	Not Used	ANC_DATA_SWITCH	STAT3_CONFIG b2	STAT3_CONFIG b1	STAT3_CONFIG b0	STAT2_CONFIG b2	STAT2_CONFIG b1	STAT2_CONFIG b0	STAT1_CONFIG b2	STAT1_CONFIG b1	STAT1_CONFIG b0	STAT0_CONFIG b2	STAT0_CONFIG b1	STAT0_CONFIG b0
DATA_FORMAT	04h	Not Used	Not Used	Not Used	Not Used	EDH_FLAG_UPDATE	AP_CRC_V	FF_CRC_V	EDH_DETECT	VERSION_352M	Not Used	Not Used	STD_LOCK	DATA_FORMAT b3	DATA_FORMAT b2	DATA_FORMAT b1	DATA_FORMAT b0
EDH_FLAG_OUT	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
EDH_FLAG_IN	02h	Not Used	ANC-UES_IN	ANC-IDA_IN	ANC-IDH_IN	ANC-EDA_IN	ANC-EDH_IN	FF-UES_IN	FF-IDA_IN	FF-IDH_IN	FF-EDA_IN	FF-EDH_IN	AP-UES_IN	AP-IDA_IN	AP-IDH_IN	AP-EDA_IN	AP-EDH_IN
ERROR_STATUS	01h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR	CCS_ERR	SAV_ERR	EAV_ERR
IOPROC_DISABLE	00h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	ANC_PKT_EXT	FIFO_MODE d1	FIFO_MODE b0	H_CONFIG	Not Used	Not Used	ILLEGAL_REMAP	EDH_CRC_INS	ANC_CSUM_INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

2.5.1 Host Interface Map (R/W registers)

Table 2-5: Host Interface Map (R/W registers)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_LD_POSITION[12:0]	28h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	27h																
	26h																
ERROR_MASK_REGISTER	25h										VD_STD_ERR_MASK	FF_CRC_ERR_MASK	AP_CRC_ERR_MASK	LOCK_ERR_MASK	CCS_ERR_MASK	SAV_ERR_MASK	EAV_ERR_MASK
FF_PIXEL_END_F1[12:0]	24h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	14h																
	13h																
	12h																
	11h																
	10h																
	0Fh																
ANC_TYPE(5)[15:0]	0Eh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(4)[15:0]	0Dh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(3)[15:0]	0Ch	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(2)[15:0]	0Bh	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE(1)[15:0]	0Ah	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_B[10:0]	09h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_EMPTY_OFFSET	06h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h				ANC_DATA_SWITCH	STAT3_CONFIG b2	STAT3_CONFIG b1	STAT3_CONFIG b0	STAT2_CONFIG b2	STAT2_CONFIG b1	STAT2_CONFIG b0	STAT1_CONFIG b2	STAT1_CONFIG b1	STAT1_CONFIG b0	STAT0_CONFIG b2	STAT0_CONFIG b1	STAT0_CONFIG b0
DATA_FORMAT	04h					EDH_FLAG_UPDATE											
	03h																
	02h																
	01h																
IOPROC_DISABLE	00h							ANC_PKT_EXT	FIFO_MODE b1	FIFO_MODE b0	H_CONFIG			ILLEGAL_REMAP	EDH_CRC_INS	ANC_CSUM_INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

2.5.2 Host Interface Map (Read only registers)

Table 2-6: Host Interface Map (Read only registers)

Register Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	28h																
	27h																
	26h																
	25h																
	24h																
	23h																
	22h																
	21h																
	20h																
	1Fh																
	1Eh																
	1Dh																
	1Ch																
	1Bh																
	1Ah																
	19h																
	18h																
	17h																
	16h																
	15h																
RASTER_STRUCTURE4[10:0]	14h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B(4,3)	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A(2,1)	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
	09h																
	08h																
	07h																
	06h																
	05h																
DATA_FORMAT	04h						AP_CRC_V	FF_CRC_V	EDH_DETECT	VERSION_352M			STD_LOCK	DATA_FORMAT b3	DATA_FORMAT b2	DATA_FORMAT b1	DATA_FORMAT b0
EDH_FLAG_OUT	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
EDH_FLAG_IN	02h	Not Used	ANC-UES_IN	ANC-IDA_IN	ANC-IDH_IN	ANC-EDA_IN	ANC-EDH_IN	FF-UES_IN	FF-IDA_IN	FF-IDH_IN	FF-EDA_IN	FF-EDH_IN	AP-UES_IN	AP-IDA_IN	AP-IDH_IN	AP-EDA_IN	AP-EDH_IN
ERROR_STATUS	01h										VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR	CCS_ERR	SAV_ERR	EAV_ERR
	00h																

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. The contents may be accessed in Ancillary Data Extraction mode (see Section 3.10.3).

3. Detailed Description

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3.1 Functional Overview

The GS9090 is a 270Mb/s reclocking deserializer with an internal FIFO and programmable multi-function output port. The device has two basic modes of operation which determine precisely how SMPTE or DVB-ASI compliant input data streams are reclocked and processed.

In Auto mode (AUTO/$\overline{\text{MAN}}$ = HIGH), the GS9090 will automatically detect, reclock, deserialize, and process SD SMPTE 259M-C, or DVB-ASI input data.

In Manual mode (AUTO/$\overline{\text{MAN}}$ = LOW), the application layer must set external device pins for the correct reception of either SMPTE or DVB-ASI data. Manual mode also supports the reclocking and deserializing of 270Mb/s data not conforming to SMPTE or DVB-ASI streams.

The digital signal processing core implements several data processing functions including error detection and correction and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI host interface.

The provided programmable multi-function output pins may be configured to output various status signals including H, V, and F timing, ancillary data detection, EDH detection, and a FIFO load pulse. The internal FIFO supports 4 modes of operation, which may be used for data alignment / delay, MPEG packet extraction, or ancillary data extraction.

The GS9090 contains a JTAG interface for boundary scan test implementations.

3.2 Serial Digital Input

The GS9090 contains a current mode differential serial digital input buffer, allowing the device to be connected to SMPTE 259M-C compliant serial digital input signals.

The input buffer has internal 50Ω termination resistors, which are connected to ground via the TERM pin. If the input signal is AC coupled to the device, the signal source common mode level will be set internally to approximately 1.45V.

3.3 Clock and Data Recovery

The output of the serial digital input buffer passes to the GS9090's internal reclocker block. The function of this block is to lock to the input data stream, extract a clean clock, and retime the serial digital data to remove high frequency jitter.

The operating centre frequency of the internal reclocker is 270Mb/s where the input jitter tolerance (IJT) is +/- 0.2UI at this rate.

If the reclocker locks to the signal, it will provide internal pll_lock and carrier_detect signals to the lock detect block of the device.

3.3.1 Internal VCO and Phase Detector

The GS9090 uses an internal VCO and PFD as part of the internal reclocker's phase-locked loop. Each block requires a +1.8V DC power supply, which is supplied via the VCO_VDD / VCO_GND and PLL_VDD / PLL_GND pins.

3.4 Serial-To-Parallel Conversion

The retimed data and phase-locked clock signals from the internal reclocker are fed to the serial-to-parallel converter. The function of this block is to extract 10-bit parallel data words from the reclocked serial data stream and simultaneously present them to the SMPTE and DVB-ASI word alignment blocks.

3.5 Modes Of Operation

The GS9090 has two basic modes of operation: Auto mode and Manual mode. Auto mode is enabled when the application layer sets the AUTO/MAN pin HIGH, and Manual mode is enabled when the AUTO/MAN pin is set LOW. As indicated in Figure 3-1, each mode supports both SMPTE and DVB-ASI input signals. In addition, Data-Through functionality is possible when the GS9090 is in Manual mode.

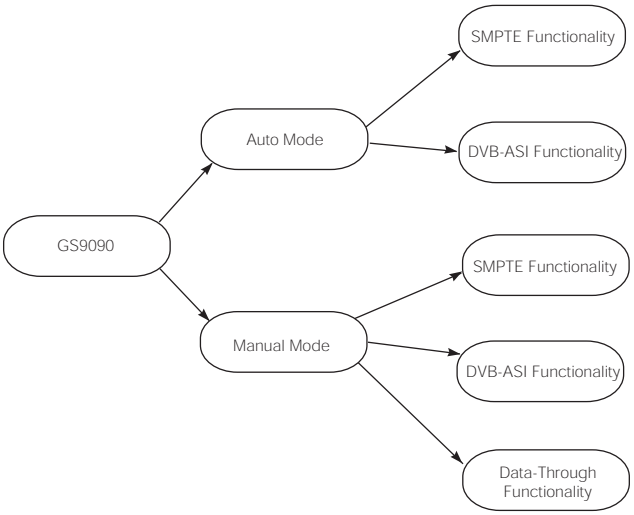


Figure 3-1: GS9090's Modes of Operation

3.5.1 Lock Detect

Once the internal reclocker has locked to the received serial digital data stream, the lock detect block of the GS9090 searches for the appropriate sync words, and indicates via the LOCKED output pin when the device has successfully achieved lock. The LOCKED pin is designed to be stable. It will not toggle during the locking process, nor will it glitch during a synchronous switch.

Lock detection is a continuous process, which begins after a system reset and continues until the device is powered down or held in reset. This process is summarized in Figure 3-2.

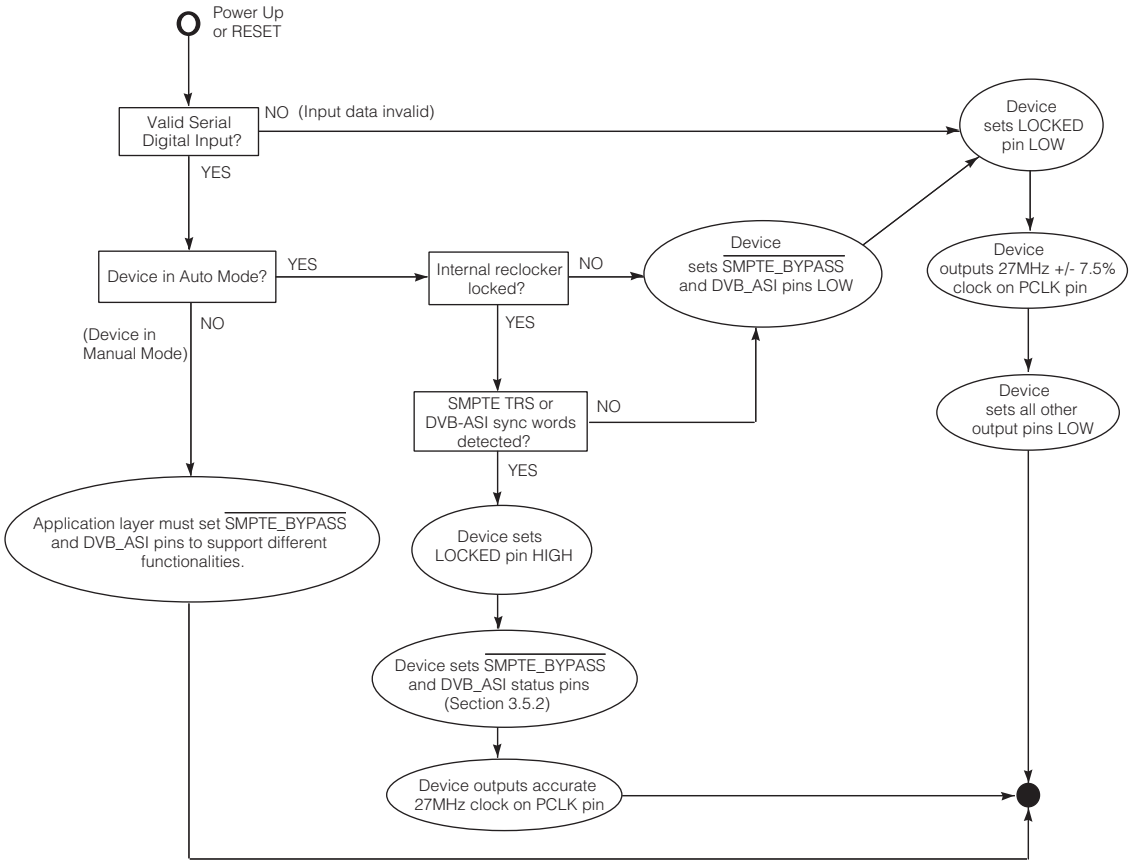


Figure 3-2: Lock Detection Process

The lock detection algorithm first determines if a valid serial digital input signal has been presented to the device by sampling the internal carrier_detect signal. When the serial data input is considered invalid the LOCKED pin will be set LOW, and all device outputs will be forced LOW, except PCLK. The PCLK output frequency will be 27MHz +/- 7.5% over the temperature range of -20°C to +85°C.

If a valid serial digital input signal has been detected, and the device is in Auto mode, the lock algorithm will attempt to detect the presence of either SMPTE TRS words or DVB-ASI sync words. Assuming that a valid 270Mb/s SMPTE or DVB-ASI signal has been applied to the device, the LOCKED pin will be set HIGH and the synchronous and asynchronous lock times will be as listed in the AC Electrical Characteristics table.

In Manual mode, the application layer must set the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins appropriately so that the lock detect block will search for either SMPTE TRS or DVB-ASI sync words. Synchronous and asynchronous lock times are also listed in the AC Electrical Characteristics table.

NOTE: The PCLK output will continue to operate at 27MHz +/- 7.5% during the lock detection process. Only when the device is locked (LOCKED = HIGH) will the PCLK output an accurate 27MHz signal.

For SMPTE and DVB-ASI inputs, the lock detect block will only assert the LOCKED output pin HIGH if (1) the reclocker has locked to the input data stream, and (2) TRS or DVB-ASI sync words have been correctly identified.

For serial inputs that do not conform to SMPTE or DVB-ASI formats, one of the following will occur once the reclocker has locked:

1. In Manual mode, data will be passed directly to the parallel outputs without any further processing taking place and the LOCKED signal will be asserted HIGH if and only if the SMPTE_BYPASS and DVB_ASI input pins are set LOW (see Data-Through functionality on page 29); or
2. In Auto mode, the LOCKED signal will be asserted LOW, the parallel outputs will be set to logic LOW, and the SMPTE_BYPASS and DVB_ASI output signals will also be set LOW.

If the internal reclocker does not lock to the input, the internal pll_lock signal will be LOW, and the lock detect block will not search for sync words. The LOCKED signal will be set LOW, and all device outputs except PCLK will be forced LOW. The PCLK output frequency will be 27MHz +/- 7.5% over the temperature range of -20°C to +85°C.

3.5.2 Auto Mode

Recall that the GS9090 is in Auto mode when the AUTO/MAN input pin is set HIGH by the application layer. In this mode, SMPTE_BYPASS and DVB_ASI become output status pins. Table 3-1 shows the status of these pins when different serial digital video signals are applied.

Table 3-1: Auto Mode Output Status Signals

	Pin Settings	
Format	**SMPTE_BYPASS**	**DVB_ASI**
SD SMPTE	HIGH	LOW
DVB-ASI	LOW	HIGH
NOT SMPTE OR DVB-ASI*	LOW	LOW

*NOTE: In this case the device will not be locked (LOCKED = LOW), and all digital output pins except PCLK will be set LOW (see Lock Detect on page 22)

3.5.3 Manual Mode

Recall that the GS9090 is in Manual mode when the AUTO/$\overline{\text{MAN}}$ input pin is set LOW by the application layer. In this mode the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins become input signals, and the application layer determines the operating mode of the device by setting these pins as shown in Table 3-2

Table 3-2: Manual Mode Input Status Signals

	Pin Settings	
Format	**$\overline{\text{SMPTE\_BYPASS}}$**	**DVB_ASI**
SD SMPTE	HIGH	LOW
DVB-ASI	X	HIGH
NOT SMPTE OR DVB-ASI (Data-Through mode)*	LOW	LOW

*NOTE: See Data-Through functionality on page 29 for more detail on Data-Through mode

3.6 SMPTE Functionality

The GS9090 enters SMPTE mode once the device has detected SMPTE TRS sync words and locked to the input data stream as described in Lock Detect on page 22. The GS9090 will remain in SMPTE mode until such time that SMPTE TRS sync words fail to be detected.

The lock detect block may also drop out of SMPTE mode under any of the following conditions:

- $\overline{\text{SMPTE\_BYPASS}}$ is asserted LOW in Manual mode
- $\overline{\text{RESET}}$ is asserted LOW
- LOCKED is LOW (i.e. the device loses lock to the input signal)

TRS word detection is a continuous process, and the device will identify both 8-bit and 10-bit TRS words.

In Auto mode, the GS9090 sets the $\overline{\text{SMPTE\_BYPASS}}$ pin HIGH and the DVB_ASI pin LOW to indicate that it has locked to a SMPTE input data stream. When operating in Manual mode, the application layer must assert the DVB_ASI pin LOW and the $\overline{\text{SMPTE\_BYPASS}}$ pin HIGH in order to enable SMPTE operation.

3.6.1 SMPTE Descrambling and Word Alignment

After serial-to-parallel conversion, the internal 10-bit data bus is fed to the SMPTE descramble and word alignment internal block. The function of this block is to carry out NRZI-to-NRZ decoding, descrambling according to SMPTE 259M-C, and word alignment of the data to the TRS sync words.

NOTE: When 8-bit data is embedded in the 10-bit SMPTE signal, the two LSBs (DOUT[1:0]) must be set to zero for word alignment to work correctly.

Word alignment occurs when two consecutive valid TRS words (SAV and EAV inclusive) with the same bit alignment have been detected (1 video line).

In normal operation, re-synchronization of the word alignment process will only take place when two consecutive identical TRS word positions have been detected. When automatic or manual switch line lock handling occurs (see Switch Line Lock Handling on page 27), word alignment re-synchronization will occur on the next received TRS code word.

The device will drop out of SMPTE mode, only after 6 consecutive missing TRS timing words.

3.6.2 Internal Flywheel

The GS9090 has an internal flywheel for the generation of internal / external timing signals, the detection and correction of certain error conditions, and the automatic detection of video standards. The flywheel is only operational in SMPTE mode.

The flywheel 'learns' the video standard by monitoring the horizontal and vertical reference information contained in the TRS ID words of the received video stream. Full synchronization of the flywheel to the received video standard therefore requires one complete video frame.

Once synchronization has been achieved, the flywheel will continue to monitor the received TRS timing information to maintain synchronization.

The FW_EN input pin controls the synchronization mechanism of the flywheel. When this input signal is LOW, the flywheel will re-synchronize all pixel and line based counters on every received TRS ID word.

When FW_EN is held HIGH, re-synchronization of the pixel and line based counters will take place after 3 consecutive video lines with identical TRS timing are identified. This provides a measure of noise immunity for output timing signal generation.

The flywheel will be disabled should the LOCKED signal or $\overline{\text{RESET}}$ signal be LOW. This will occur regardless of the setting of the FW_EN pin.

3.6.3 Switch Line Lock Handling

The principle of switch line lock handling is that the switching of synchronous video sources will only disturb the horizontal timing and alignment of the stream, whereas the vertical timing remains in synchronization.

To account for the horizontal disturbance caused by a synchronous switch, it is necessary to re-synchronize the flywheel immediately after the switch has taken place. Rapid re-synchronization of the GS9090 to the new video standard can be achieved by controlling the flywheel using the FW_EN pin.

At every PCLK cycle the device samples the FW_EN pin. When the FW_EN pin is set LOW anywhere within the active line, the flywheel will re-synchronize immediately to the next TRS word.

The ability to manually re-synchronize the flywheel is also important when switching asynchronous sources or to implement other non-standardized video switching functions.

The GS9090 also implements automatic switch line lock handling. By utilizing both the synchronous switch point defined in SMPTE RP168, and the automatic video standards detect function, the device automatically re-synchronizes the flywheel at the switch point. This will occur whether or not the device has detected TRS word errors. Word alignment re-synchronization will also take place at this time.

Automatic switch line lock handling will occur regardless of the setting of the FW_EN pin.

The switch line is as defined in Table 3-3.

Table 3-3: Switch Line Position for 270Mb/s Digital Systems

System	Video Format	Sampling	Signal Standard	Parallel Interface	Serial Interface	Switch Line Number
525	720x483/59.94 (2:1)	4:2:2	125M	125M	259M-C	10, 273
625	720x576/50 (2:1)	4:2:2	BT.656	125M	259M-C	6, 319

3.6.4 HVF Timing Signal Generation

The GS9090 extracts critical timing parameters from either the received TRS signals (FW_EN = LOW) or from the internal flywheel-timing generator (FW_EN = HIGH).

Horizontal blanking period (H), vertical blanking period (V), and field odd / even timing (F) are extracted and are available for output on any of the multi-function output port pins, if so programmed (see Programmable Multi-Function Outputs on page 56).

The H signal timing is configurable via the H_CONFIG bit of the internal IOPROC_DISABLE register as either active line-based blanking, or TRS-based blanking (see Table 3-14 in Error Correction and Insertion on page 43).

The default setting of this bit (after $\overline{\text{RESET}}$ has been asserted) is LOW.

Active line-based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H output is HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing used by the device.

When H_CONFIG is set HIGH, TRS based blanking is enabled. In this case, the H output will be HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words.

The timing of these signals is shown in Figure 3-3.

NOTE 1: When the internal FIFO is configured for video mode, the H, V, and F signals will be timed to the data output from the FIFO (see Video Mode on page 46).

NOTE 2: When the GS9090 is configured for Low-latency mode, the H, V, and F output timing will be TRS-based only as shown in GS9090 Low-latency Mode on page 58. Active line-based timing is not available in this mode, and the setting of the H_CONFIG host interface bit will be ignored.

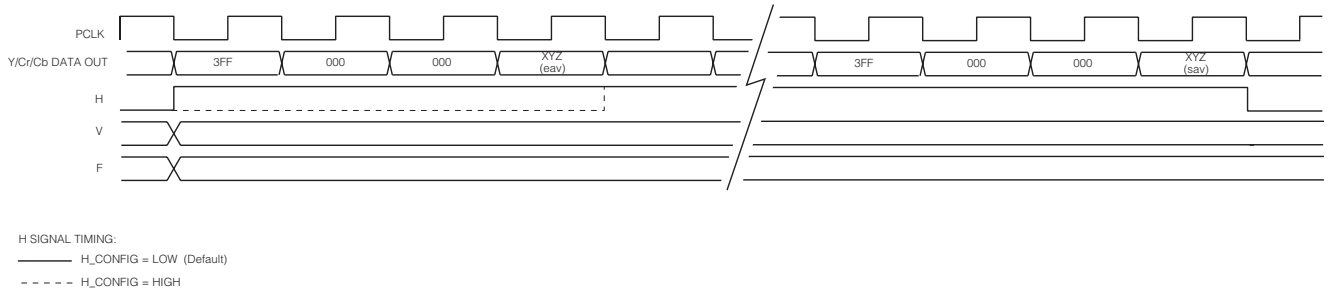


Figure 3-3: H,V,F Timing

3.7 DVB-ASI Functionality

The GS9090 enters DVB-ASI mode once the device has detected 32 consecutive DVB-ASI words without a single word or disparity error being generated. The device will remain in DVB-ASI mode until 32 consecutive DVB-ASI words or disparity errors are detected, or until SMPTE TRS ID words have been detected.

The lock detect block may also drop out of DVB-ASI mode under the following conditions:

- $\overline{\text{RESET}}$ is asserted LOW
- Both AUTO/$\overline{\text{MAN}}$ and DVB_ASI are asserted LOW
- LOCKED pin is LOW (i.e. the device loses lock to the input signal)

K28.5 sync patterns in the received DVB-ASI data stream will be detected by the device in either inverted or non-inverted form.

In Auto mode, the GS9090 sets the $\overline{\text{SMPTE\_BYPASS}}$ pin LOW and the DVB_ASI pin HIGH to indicate that it has locked to a DVB-ASI input data stream. When operating in Manual mode, the application layer must set the DVB_ASI pin HIGH to enable DVB-ASI operation. The $\overline{\text{SMPTE\_BYPASS}}$ pin will be ignored.

3.7.1 DVB-ASI 8b/10b Decoding

After serial-to-parallel conversion, the internal 10-bit data bus is fed to the DVB-ASI 8b/10b decode and word alignment block. The function of this block is to word align the data to the K28.5 sync characters, and 8b/10b decode and bit-swap the data to achieve bit alignment with the data outputs.

The extracted 8-bit data will be presented to DOUT [7:0], bypassing all internal SMPTE mode data processing.

3.7.2 Status Signal Outputs

In DVB-ASI mode, the DOUT9 and DOUT8 pins will be configured as DVB-ASI status signals WORDERR and SYNCOUT respectively.

SYNCOUT will be HIGH whenever a K28.5 sync character is present on the output. WORDERR will be HIGH whenever the device has detected an illegal code word or there is a running disparity error.

3.8 Data-Through functionality

The GS9090 may be configured by the application layer to operate as a simple serial-to-parallel converter. In this mode, the device presents data to the output data bus without performing any decoding, descrambling, or word-alignment.

Data-Through functionality is enabled only when the application layer sets the AUTO/$\overline{\text{MAN}}$, $\overline{\text{SMPTE\_BYPASS}}$, and DVB_ASI input pins LOW. Under these conditions, the lock detect block allows 270Mb/s input data not conforming to SMPTE or DVB-ASI streams to be reclocked and deserialized. If the device is in

Data-Through mode, and the internal reclocker locks to the data stream, the LOCKED pin will be set HIGH.

If the application layer does not set the AUTO/MAN pin LOW, the GS9090 will set the SMPTE_BYPASS and DVB_ASI signals to logic LOW if presented with a data stream without SMPTE TRS ID words or DVB-ASI sync words. In addition, the LOCKED pin and data bus output pins will be forced LOW.

3.9 Additional Processing Features

The GS9090 contains additional processing features that are available in SMPTE mode only (see SMPTE Functionality on page 25).

3.9.1 FIFO Load Pulse

To aid in the implementation of auto-phasing and line synchronization functions, the GS9090 will generate a FIFO load pulse to reset line-based FIFO storage. This FIFO_LD signal is available for output on one of the multi-function output port pins, if so programmed (see Programmable Multi-Function Outputs on page 56).

The FIFO_LD pulse will normally be HIGH, but will go LOW for one PCLK period, thereby generating a FIFO write reset signal.

By default, the FIFO load pulse will be generated such that it is co-timed to the SAV XYZ code word presented to the output data bus. This co-timing ensures that the next PCLK cycle will correspond with the first active sample of the video line.

NOTE: When the internal FIFO of the GS9090 is set to operate in video mode, the FIFO_LD pulse can be used to drive the RD_RESET input to the device (see Video Mode on page 46).

Figure 3-4 shows the default timing relationship between the FIFO_LD signal and the output video data.

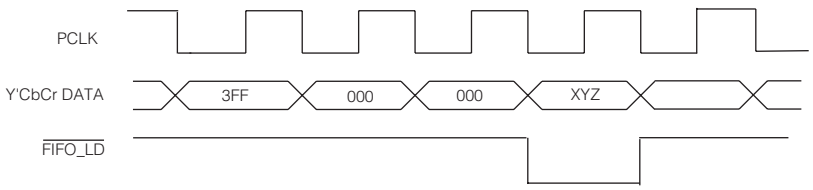


Figure 3-4: FIFO_LD Pulse Timing

3.9.1.1 Programmable FIFO Load Position

The position of the FIFO_LD pulse can be moved in PCLK increments from its default position to a maximum of one full line. The offset number of PCLK's must be programmed in the FIFO_LD_POSITION[12:0] internal register (address 28h), via the host interface.

The FIFO_LD_POSITION[12:0] register is designed to accommodate the longest SD line length. If the user programs a value greater than the maximum line length at the operating SD standard, the FIFO_LD pulse will not be generated.

After a device reset, the FIFO_LD_POSITION[12:0] register is set to zero and the FIFO_LD pulse will assume the default timing.

3.9.2 Ancillary Data Detection and Indication

The GS9090 will detect all types of ancillary data in either the vertical or horizontal data spaces. The ANC_DETECT status signal is provided to indicate the position of ancillary data in the output data stream. This signal is available for output on the multi-function output port pins, if so programmed (see Programmable Multi-Function Outputs on page 56).

The ANC_DETECT status signal is synchronous with PCLK and can be used as a clock enable to external logic, or as a write enable to an external FIFO or other memory device. The ANC_DETECT signal will be asserted HIGH whenever ancillary data is detected in the video data stream (see Figure 3-5). Both 8-bit and 10-bit ancillary data preambles will be detected by the GS9090.

NOTE 1: When the internal FIFO is configured for video mode, the ANC_DETECT signal will be timed to the data output from the FIFO (see Video Mode on page 46).

NOTE 2: For performance in low latency mode, see GS9090 Low-latency Mode on page 58.

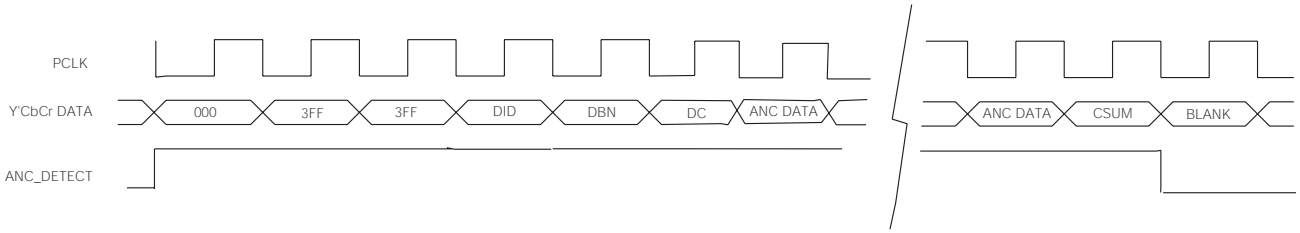


Figure 3-5: ANC_DETECT Status Signal

3.9.2.1 Programmable Ancillary Data Detection

Although the GS9090 will detect all types of ancillary data by default, it also allows the application layer to specifically program up to five different ancillary data types for detection. This is accomplished by setting the ANC_TYPE registers via the host interface (see Table 3-4).

For each data type to be detected, the host interface must program the DID and/or SDID of the ancillary data type of interest. The GS9090 will compare the received DID and/or SDID with the programmed values and assert ANC only if an exact match is found. The same timing shown in Figure 3-5 will be used.

If any DID or SDID value is set to zero in the ANC_TYPE register, no comparison or match will be made for that value. For example, if the DID is programmed but the SDID is set to zero, the device will detect all ancillary data types matching the DID value, regardless of the SDID. If both DID and SDID values are non-zero, then the received ancillary data type must match both the DID and SDID cases before the device will assert ANC_DETECT HIGH.

In the case where all five DID and SDID values are set to zero, the GS9090 will detect all ancillary data types. This is the default setting after a device reset.

Where one or more, but less than five, DID and/or SDID values have been programmed, then only those matching ancillary data types will be detected and indicated.

NOTE: See SMPTE 291M for a definition of ancillary data terms.

Table 3-4: Host Interface Description for Programmable Ancillary Data Type registers

Register Name	Bit	Name	Description	R/W	Default
ANC_TYPE 1 Address: 0Ah	15-8	ANC_TYPE1[15:8]	Used to program the DID for ancillary data detection at ANC_DETECT output	R/W	0
	7-0	ANC_TYPE1[7:0]	Used to program the SDID for ancillary data detection at ANC_DETECT output. Should be set to zero if no SDID is present in the ancillary data packet to be detected.	R/W	0
ANC_TYPE 2 Address: 0Bh	15-8	ANC_TYPE2[15:8]	Used to program the DID for ancillary data detection at ANC_DETECT output	R/W	0
	7-0	ANC_TYPE2[7:0]	Used to program the SDID for ancillary data detection at ANC_DETECT output. Should be set to zero if no SDID is present in the ancillary data packet to be detected.	R/W	0
ANC_TYPE 3 Address: 0Ch	15-8	ANC_TYPE3[15:8]	Used to program the DID for ancillary data detection at ANC_DETECT output	R/W	0
	7-0	ANC_TYPE3[7:0]	Used to program the SDID for ancillary data detection at ANC_DETECT output. Should be set to zero if no SDID is present in the ancillary data packet to be detected.	R/W	0
ANC_TYPE 4 Address: 0Dh	15-8	ANC_TYPE4[15:8]	Used to program the DID for ancillary data detection at ANC_DETECT output	R/W	0
	7-0	ANC_TYPE4[7:0]	Used to program the SDID for ancillary data detection at ANC_DETECT output. Should be set to zero if no SDID is present in the ancillary data packet to be detected.	R/W	0
ANC_TYPE 5 Address: 0Eh	15-8	ANC_TYPE5[15:8]	Used to program the DID for ancillary data detection at ANC_DETECT output	R/W	0
	7-0	ANC_TYPE5[7:0]	Used to program the SDID for ancillary data detection at ANC_DETECT output. Should be set to zero if no SDID is present in the ancillary data packet to be detected.	R/W	0

3.9.3 EDH Packet Detection

The GS9090 will determine if EDH packets are present in the incoming video data and assert the EDH_DETECT output status signal appropriately.

EDH_DETECT will be set HIGH when EDH packets have been detected and will remain HIGH until EDH packets are no longer present. The signal will be set LOW at the end of the vertical blanking (falling edge of V) if an EDH packet has not been received and detected during vertical blanking.

EDH_DETECT is available for output on the multi-function output port pins, if so programmed (see Programmable Multi-Function Outputs on page 56). Additionally, the EDH_DETECT bit is stored in the DATA_FORMAT register at address 04h (see Table 3-7).

3.9.4 EDH Flag Detection

As described in EDH Packet Detection on page 33, the GS9090 can detect EDH packets in the received data stream. The EDH flags for ancillary data, active picture, and full field areas are extracted from the detected EDH packets and placed in the EDH_FLAG_IN register of the device (Table 3-5).

When the EDH_FLAG_UPDATE bit in the DATA_FORMAT register (Table 3-7) is set HIGH by the application layer, the GS9090 will update the ancillary data, full field, and active picture EDH flags according to SMPTE RP165. The updated EDH flags are placed in the EDH_FLAG_OUT register (Table 3-6). The EDH packet output from the device will contain the updated flags.

One set of flags is provided for both fields 1 and 2. Field 1 flag data will be overwritten by field 2 flag data.

When no EDH packets are detected (EDH_DETECT = LOW), the UES flags in the EDH_FLAG_OUT register will be set HIGH to signify that the received signal does not support the error detection practice. These flags are set regardless of the setting of the EDH_FLAG_UPDATE bit.

NOTE: When EDH_FLAG_UPDATE is LOW with EDH packets in the video stream, the content of the EDH_FLAG_OUT register is not valid and should be ignored.

Both EDH_FLAG registers may be read by the host interface at any time during the received frame except on the lines defined in SMPTE RP165 where these flags are updated.

The GS9090 will also extract the CRC valid or ‘V’ bit for both active picture and full field CRCs. The AP_CRC_V bit in the DATA_FORMAT register provides the active picture CRC valid bit status, and the FF_CRC_V bit provides the full field CRC valid bit status (see Table 3-7). When EDH_DETECT = LOW, these bits will be cleared.

The flag register values remain set until overwritten by the decoded flags in the next received EDH packet in the following field. When no EDH packet is detected during vertical blanking, the flag registers will be cleared at the end of the vertical blanking period.

Table 3-5: Host Interface Description for EDH Flag Registers

Register Name	Bit	Name	Description	R/W	Default
EDH_FLAG_IN Address: 02h	15	–	Not Used	–	–
	14	ANC-UES_IN	Ancillary Unknown Error Status Flag	R	0
	13	ANC-IDA_IN	Ancillary Internal device error Detected Already Flag.	R	0
	12	ANC-IDH_IN	Ancillary Internal device error Detected Here Flag.	R	0
	11	ANC-EDA_IN	Ancillary Error Detected Already Flag.	R	0
	10	ANC-EDH_IN	Ancillary Error Detected Here Flag.	R	0
	9	FF-UES_IN	Full Field Unknown Error Status Flag.	R	0
	8	FF-IDA_IN	Full Field Internal device error Detected Already Flag.	R	0
	7	FF-IDH_IN	Full Field Internal device error Detected Here Flag.	R	0
	6	FF-EDA_IN	Full Field Error Detected Already Flag.	R	0
	5	FF-EDH_IN	Full Field Error Detected Here Flag.	R	0
	4	AP-UES_IN	Active Picture Unknown Error Status Flag.	R	0
	3	AP-IDA_IN	Active Picture Internal device error Detected Already Flag.	R	0
	2	AP-IDH_IN	Active Picture Internal device error Detected Here Flag	R	0
	1	AP-EDA_IN	Active Picture Error Detected Already Flag.	R	0
	0	AP-EDH_IN	Active Picture Error Detected Here Flag.	R	0

Table 3-6: Host Interface Description for EDH Flag Registers

Register Name	Bit	Name	Description	R/W	Default
EDH_FLAG_OUT Address: 03h	15	–	Not Used	–	–
	14	ANC-UES	Ancillary Unknown Error Status Flag	R	0
	13	ANC-IDA	Ancillary Internal device error Detected Already Flag.	R	0
	12	ANC-IDH	Ancillary Internal device error Detected Here Flag.	R	0
	11	ANC-EDA	Ancillary Error Detected Already Flag.	R	0
	10	ANC-EDH	Ancillary Error Detected Here Flag.	R	0
	9	FF-UES	Full Field Unknown Error Status Flag.	R	0
	8	FF-IDA	Full Field Internal device error Detected Already Flag.	R	0
	7	FF-IDH	Full Field Internal device error Detected Here Flag.	R	0
	6	FF-EDA	Full Field Error Detected Already Flag.	R	0
	5	FF-EDH	Full Field Error Detected Here Flag.	R	0
	4	AP-UES	Active Picture Unknown Error Status Flag.	R	0
	3	AP-IDA	Active Picture Internal device error Detected Already Flag.	R	0
	2	AP-IDH	Active Picture Internal device error Detected Here Flag	R	0
	1	AP-EDA	Active Picture Error Detected Already Flag.	R	0
	0	AP-EDH	Active Picture Error Detected Here Flag.	R	0

Table 3-7: Host Interface Description for Data Format Register

Register Name	Bit	Name	Description	R/W	Default
DATA_FORMAT Address: 04h	15-12	–	Not Used	–	–
	11	EDH_FLAG_UPDATE	When set HIGH by the application layer, the device will update the ancillary data, full field, and active picture EDH flags according to SMPTE RP165.	R/W	0
	10	AP_CRC_V	Active Picture CRC Valid bit.	R	0
	9	FF_CRC_V	Full Field CRC Valid bit.	R	0
	8	EDH_DETECT	Set HIGH by the device when EDH packets are detected in the incoming video data.	R	0
	7	VERSION_352M	Indicates whether decoded SMPTE 352M packet is version 0 or version 1. See SMPTE 352M Payload Identifier on page 36.	R	0
	6-5	–	Not Used	–	–
	4	STD_LOCK	Standard Lock bit. This bit will be set HIGH when the flywheel has achieved full synchronization to the received video standard. See Automatic Video Standard and Data Format Detection on page 37.	R	0
	3-0	DATA_FORMAT[3:0]	Displays the data format being carried on the serial digital interface. See Video Standard Indication on page 38.	R	0

3.9.5 SMPTE 352M Payload Identifier

The GS9090 can receive and detect the presence of the SMPTE 352M payload identifier ancillary data packet. This four word payload identifier packet may be used to indicate the transport mechanism, frame rate and line scanning / sampling structure.

Upon reception of this packet, the device will extract the four words describing the video format being transported and make this information available to the host interface via the four VIDEO_FORMAT 8 bit registers (Table 3-8). The device will also indicate the version of the payload packet in bit 7 of the DATA_FORMAT register (Table 3-7). When this bit is set HIGH the received SMPTE 352M packet is version 1, otherwise it is version 0.

The VIDEO_FORMAT registers will only be updated if the received checksum is the same as the locally calculated checksum.

NOTE: The VIDEO_FORMAT registers will not be updated with 352M payload data if the packets are not on the correct video line (as stated in this standard).

These registers will be cleared to zero, indicating an undefined format, if the device loses lock to the input data stream (LOCKED = LOW), or if the $\overline{\text{SMPTE\_BYPASS}}$ pin is asserted LOW. This is also the default setting after a device reset.

Table 3-8: Host Interface Description for SMPTE 352M Payload Identifier Registers

Register Name	Bit	Name	Description	R/W	Default
VIDEO_FORMAT_OUT_B Address: 10h	15-8	SMPTE 352M Byte 4	Data will be available in this register when Video Payload Identification Packets are detected in the data stream.	R	0
	7-0	SMPTE 352M Byte 3	Data will be available in this register when Video Payload Identification Packets are detected in the data stream.	R	0
VIDEO_FORMAT_OUT_A Address: 0Fh	15-8	SMPTE 352M Byte 2	Data will be available in this register when Video Payload Identification Packets are detected in the data stream.	R	0
	7-0	SMPTE 352M Byte 1	Data will be available in this register when Video Payload Identification Packets are detected in the data stream.	R	0

3.9.6 Automatic Video Standard and Data Format Detection

The GS9090 can independently detect the input video standard and data format by using the timing parameters extracted from the received TRS ID words. Total samples per line, active samples per line, total lines per field/frame, and active lines per field/frame are all calculated and presented to the host interface via the RASTER_STRUCTURE registers (Table 3-9).

Also associated with the RASTER_STRUCTURE registers is the status bit, STD_LOCK. The GS9090 will set STD_LOCK HIGH when the flywheel has achieved full synchronization to the received video standard. STD_LOCK is stored in the DATA_FORMAT register (Table 3-7).

The four RASTER_STRUCTURE registers, as well as the STD_LOCK status bit will default to zero after a device reset. They will also default to zero if the device loses lock to the input data stream (LOCKED = LOW), or if the $\overline{\text{SMPTE\_BYPASS}}$ pin is asserted LOW.

Table 3-9: Host Interface Description for Raster Structure Registers

Register Name	Bit	Name	Description	R/W	Default
RASTER_STRUCTURE1 Address: 11h	15-11	–	Not Used	–	–
	10-0	RASTER_STRUCTURE1[10:0]	Total Lines Per Frame	R	0
RASTER_STRUCTURE2 Address: 12h	15-13	–	Not Used	–	–
	12-0	RASTER_STRUCTURE2[12:0]	Total Words Per Line	R	0
RASTER_STRUCTURE3 Address: 13h	15-13	–	Not Used	–	–
	12-0	RASTER_STRUCTURE3[12:0]	Words Per Active Line	R	0
RASTER_STRUCTURE4 Address: 14h	15-11	–	Not Used	–	–
	10-0	RASTER_STRUCTURE4[10:0]	Active Lines Per Field	R	0

3.9.6.1 Video Standard Indication

As well as detecting the video standard, the GS9090 can extract the data format being carried on the serial digital interface (i.e. SDTI, SDI, or DVB-ASI).

This information is represented by bits 0 to 3 of the DATA_FORMAT register (Table 3-7), which may be read by the application layer via the host interface. DATA_FORMAT[3:0] register codes are shown in Table 3-10.

The DATA_FORMAT[3:0] register defaults to Fh (undefined) after a system reset. The register will also be set to its default value if the device is not locked (LOCKED = LOW), or if both $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins are LOW.

Table 3-10: Data Format Register Codes

Data Format[3:0]	Data Format	Applicable Standards
0h	SDTI DVCPRO - No ECC	SMPTE 321M
1h	SDTI DVCPRO - ECC	SMPTE 321M
2h	SDTI DVCAM	SMPTE 322M
3h	SDTI CP	SMPTE 326M
4h	Other SDTI fixed block size	–
5h	Other SDTI variable block size	–
6h	SDI	–
7h	DVB-ASI	–
8h ~ Eh	Reserved	–
Fh	Unknown data format	–

3.9.7 Error Detection and Indication

The GS9090 contains a number of error detection functions to enhance operation of the device when operating in SMPTE mode. These functions, except lock error detection, will not be available in DVB-ASI mode (DVB-ASI Functionality on page 29) or Data-Through mode (Data-Through functionality on page 29).

The device maintains an error status register at address 01h called ERROR_STATUS. Each type of error has a specific flag or bit in this register that is set HIGH whenever that error is detected (Table 3-11).

All bits in the ERROR_STATUS register, except the LOCK_ERR bit, will be cleared at the start of each video field or when read by the host interface, whichever condition occurs first.

All bits, with the exception of the LOCK_ERR, will also be cleared if a change in the video standard is detected, or under the following conditions:

- LOCKED is asserted LOW
- SMPTE_BYPASS is asserted LOW in Manual mode

The whole ERROR_STATUS register, including the LOCK_ERR bit, will be set LOW during a system reset (RESET = LOW).

In addition to the ERROR_STATUS register, a register called ERROR_MASK is included to select the specific error conditions that will be detected (Table 3-12). There is one bit in the ERROR_MASK register for each type of error represented in the ERROR_STATUS register.

The bits of the ERROR_MASK register will default to '0' after a device reset, thus allowing all error types to be detected. The host interface may disable individual error detection by setting the corresponding bit HIGH in this register.

Error conditions are also indicated to the application layer via the status signal pin DATA_ERROR. This output pin is an inverted logical 'OR'ing of each error status flag stored in the ERROR_STATUS register. DATA_ERROR is normally HIGH, but will be set LOW by the device when an error condition that has not been masked is detected.

Table 3-11: Host Interface Description for Error Status Register

Register Name	Bit	Name	Description	R/W	Default
ERROR_STATUS Address: 01h	15-7	–	Not Used	–	–
	6	VD_STD_ERR	Video Standard Error Flag. Set HIGH when a mismatch between the received SMPTE 352M packets (version 1 or version 0) and the calculated video standard occurs.	R	0
	5	FF_CRC_ERR	Full Field CRC Error Flag. Set HIGH when a Full Field (FF) CRC mismatch has been detected in Field 1 or 2	R	0
	4	AP_CRC_ERR	Active Picture CRC Error Flag. Set HIGH when an Active Picture (AP) CRC mismatch has been detected in Field 1 or 2.	R	0
	3	LOCK_ERR	Lock Error Flag. Set HIGH whenever the LOCKED pin is LOW (indicating the device is not correctly locked).	R	0
	2	CS_ERR	Checksum Error Flag. Set HIGH when ancillary data packet checksum error has been detected.	R	0
	1	SAV_ERR	Start of Active Video Error Flag. Set HIGH when TRS errors are detected in either 8-bit or 10-bit TRS words.	R	0
	0	EAV_ERR	End of Active Video Error Flag. Set HIGH when TRS errors are detected in either 8-bit or 10-bit TRS words.	R	0

Table 3-12: Host Interface Description for Error Mask Register

Register Name	Bit	Name	Description	R/W	Default
ERROR_MASK Address: 25h	15-7	–	Not Used	–	–
	6	VD_STD_ERR_MASK	Video Standard Error Flag Mask bit.	R/W	0
	5	FF_CRC_ERR_MASK	Full Field CRC Error Flag Mask bit.	R/W	0
	4	AP_CRC_ERR_MASK	Active Picture CRC Error Flag Mask bit	R/W	0
	3	LOCK_ERR_MASK	Lock Error Flag Mask bit.	R/W	0
	2	CS_ERR_MASK	Checksum Error Flag Mask bit.	R/W	0
	1	SAV_ERR_MASK	Start of Active Video Error Flag Mask bit.	R/W	0
	0	EAV_ERR_MASK	End of Active Video Error Flag Mask bit.	R/W	0

3.9.7.1 Video Standard Error Detection

If a mismatch between the received SMPTE 352M packets and the calculated video standard occurs, the GS9090 will indicate a video standard error by setting the VD_STD_ERR bit of the ERROR_STATUS register HIGH. The device will detect errors in both version 1 and version 0 352M packets.

3.9.7.2 EDH CRC Error Detection

The GS9090 calculates the Full Field (FF) and Active Picture (AP) CRC words according to SMPTE RP165 in support of Error Detection and Handling packets in SD signals.

These calculated CRC values are compared with the received CRC values. If a mismatch is detected, the error is flagged in the AP_CRC_ERR and/or FF_CRC_ERR bits of the ERROR_STATUS register. These two flags are shared between fields 1 and 2.

The AP_CRC_ERR bit will be set HIGH when an active picture CRC mismatch has been detected in field 1 or 2. The FF_CRC_ERR bit will be set HIGH when a full field CRC mismatch has been detected in field 1 or 2.

EDH CRC errors will only be indicated when the device has correctly received EDH packets.

SMPTE RP165 specifies the calculation ranges and scope of EDH data for standard 525 and 625 component digital interfaces. The GS9090 will utilize these standard ranges by default.

If the received video format does not correspond to 525 or 625 digital component video standards as determined by the flywheel pixel and line counters, then one of two schemes for determining the EDH calculation ranges will be employed:

1. Ranges will be based on the line and pixel ranges programmed by the host interface; or
2. In the absence of user-programmed calculation ranges, ranges will be determined from the received TRS timing information.

The registers available to the host interface for programming EDH calculation ranges include active picture and full field line/pixel start and end positions for both fields. Table 3-13 shows the relevant registers, which default to '0' after a device reset.

If any or all of these register values are zero, then the EDH CRC calculation ranges will be determined from the flywheel generated timing. The first active and full field pixel will always be the first pixel after the SAV TRS code word. The last active and full field pixel will always be the last pixel before the start of the EAV TRS code words.

Table 3-13: Host Interface Description for EDH Calculation Range Registers

Register Name	Bit	Name	Description	R/W	Default
AP_LINE_START_F0 Address: 15h	15-11	–	Not Used	–	–
	10-0	AP_LINE_START_F0[10:0]	Field 0 Active Picture start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_END_F0 Address: 16h	15-11	–	Not Used	–	–
	10-0	AP_LINE_END_F0[10:0]	Field 0 Active Picture end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_START_F1 Address: 17h	15-11	–	Not Used	–	–
	10-0	AP_LINE_START_F1[10:0]	Field 1 Active Picture start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_END_F1 Address: 18h	15-11	–	Not Used	–	–
	10-0	AP_LINE_END_F1[10:0]	Field 1 Active Picture end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_START_F0 Address: 19h	15-11	–	Not Used	–	–
	10-0	FF_LINE_START_F0[10:0]	Field 0 Full Field start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_END_F0 Address: 1Ah	15-11	–	Not Used	–	–
	10-0	FF_LINE_END_F0[10:0]	Field 0 Full Field end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0

Table 3-13: Host Interface Description for EDH Calculation Range Registers (Continued)

Register Name	Bit	Name	Description	R/W	Default
FF_LINE_START_F1 Address: 1Bh	15-11	–	Not Used	–	–
	10-0	FF_LINE_START_F1[10:0]	Field 1 Full Field start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_END_F1 Address: 1Ch	15-11	–	Not Used	–	–
	10-0	FF_LINE_END_F1[10:0]	Field 1 Full Field end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_PIXEL_START_F0 Address: 1Dh	15-13	–	Not Used	–	–
	12-0	AP_PIXEL_START_F0[12:0]	Field 0 Active Picture start pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_PIXEL_END_F0 Address: 1Eh	15-13	–	Not Used	–	–
	12-0	AP_PIXEL_END_F0[12:0]	Field 0 Active Picture end pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_PIXEL_START_F1 Address: 1Fh	15-13	–	Not Used	–	–
	12-0	AP_PIXEL_START_F1[12:0]	Field 1 Active Picture start pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_PIXEL_END_F1 Address: 20h	15-13	–	Not Used	–	–
	12-0	AP_PIXEL_END_F1[12:0]	Field 1 Active Picture end pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_PIXEL_START_F0 Address: 21h	15-13	–	Not Used	–	–
	12-0	FF_PIXEL_START_F0[12:0]	Field 0 Full Field start pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_PIXEL_END_F0 Address: 22h	15-13	–	Not Used	–	–
	12-0	FF_PIXEL_END_F0[12:0]	Field 0 Full Field end pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_PIXEL_START_F1 Address: 23h	15-13	–	Not Used	–	–
	12-0	FF_PIXEL_START_F1[12:0]	Field 1 Full Field start pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_PIXEL_END_F1 Address: 24h	15-13	–	Not Used	–	–
	12-0	FF_PIXEL_END_F1[12:0]	Field 1 Full Field end pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0

3.9.7.3 Lock Error Detection

The LOCKED pin of the GS9090 indicates the lock status of the internal reclocker and lock detect blocks of the device. Only when the LOCKED pin is asserted HIGH has the device correctly locked to the received data stream (see Lock Detect on page 22).

The GS9090 will also indicate lock error to the host interface when LOCKED = LOW by setting the LOCK_ERR bit in the ERROR_STATUS register HIGH.

3.9.7.4 Ancillary Data Checksum Error Detection

The GS9090 will calculate checksums for all received ancillary data and compare the calculated values to the received checksum words. If a mismatch is detected, the CS_ERR bit of the ERROR_STATUS register will be set HIGH.

Although the GS9090 will calculate and compare checksum values for all ancillary data types by default, the host interface may program the device to check only certain types of ancillary data checksums. This is accomplished via the ANC_TYPE registers as described in Programmable Ancillary Data Detection on page 31.

3.9.7.5 TRS Error Detection

TRS error flags are generated by the GS9090 when:

1. The received TRS H timing does not correspond to the internal flywheel timing; or
2. The received TRS hamming codes are incorrect.

Both 8-bit and 10-bit SAV and EAV TRS words are checked for timing and data integrity errors. These are flagged via the SAV_ERR and/or EAV_ERR bits of the ERROR_STATUS register.

NOTE: H timing based TRS errors will only be generated if the FW_EN pin is set HIGH. F & V timing errors are not detected or corrected.

3.9.8 Error Correction and Insertion

In addition to signal error detection and indication, the GS9090 may also correct certain types of errors by inserting corrected code words, checksums, and TRS values into the data stream. These features are only available in SMPTE mode and the IOPROC_EN pin must be set HIGH by the application layer. Individual correction features may be enabled or disabled by setting bits 0 to 3 in the IOPROC_DISABLE register (Table 3-14).

All of the IOPROC_DISABLE register bits default to '0' after a device reset, enabling all of the processing features. To disable any individual error correction feature, the host interface must set the corresponding bit HIGH in the IOPROC_DISABLE register.

Table 3-14: Host Interface Description for Internal Processing Disable Register

Register Name	Bit	Name	Description	R/W	Default
IOPROC_DISABLE Address: 00h	15-10	–	Not Used	–	–
	9	ANC_PKT_EXT	Ancillary Packet Extraction. When the FIFO is configured for Ancillary Data Extraction mode, the application layer must set this bit HIGH to begin extraction. NOTE: Setting ANC_PKT_EXT LOW will not automatically disable ancillary data extraction (see Ancillary Data Extraction and Reading on page 51).	R/W	0
	8-7	FIFO_MODE[1:0]	FIFO Mode: These bits control which mode the internal FIFO is operating in (see Table 3-15)	R/W	0
	6	H_CONFIG	Horizontal sync timing output configuration. Set LOW for active line blanking timing. Set HIGH for H blanking based on the H bit setting of the TRS word. See Figure 3-3 in HVF Timing Signal Generation on page 28.	R/W	0
	5-4		Not Used.		
	3	ILLEGAL_REMAP	Illegal Code re-mapping. Correction of illegal code words within the active picture. Set HIGH to disable. The IOPROC_EN pin must be set HIGH.	R/W	0
	2	EDH_CRC_INS	Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error correction insertion. Set HIGH to disable. The IOPROC_EN pin must be set HIGH.	R/W	0
	1	ANC_CSUM_INS	Ancillary Data Checksum insertion. Set HIGH to disable. The IOPROC_EN pin must be set HIGH.	R/W	0
	0	TRS_INS	Timing Reference Signal Insertion. The device will correct TRS based errors when set LOW (see TRS Error Correction on page 45). The IOPROC_EN pin must also be HIGH. Set this bit HIGH to disable.	R/W	0

3.9.8.1 Illegal Code Remapping

If the ILLEGAL_REMAP bit of the IOPROC_DISABLE register is set LOW, the GS9090 will remap all codes within the active picture between the values 3FCh and 3FFh to 3FBh. All codes within the active picture area between the values 00h and 03h will be re-mapped to 04h.

In addition, 8-bit TRS and ancillary data preambles will be remapped to 10-bit values if this feature is enabled.

3.9.8.2 EDH CRC Error Correction

If the EDH_CRC_INS bit of the IOPROC_DISABLE register is set LOW, the GS9090 will generate and insert active picture and full field CRC words into the EDH data packets received by the device.

Additionally, when EDH_CRC_INS is LOW, the device will set the active picture and full field CRC 'V' bits HIGH in the EDH packet (see EDH Flag Detection on page 33). The AP_CRC_V and FF_CRC_V register bits will only report the received EDH validity flags.

EDH CRC calculation ranges are described in EDH CRC Error Detection on page 40.

NOTE: Although the GS9090 will modify and insert EDH CRC words and EDH packet checksums, the device will only update EDH error flags when the EDH_FLAG_UPDATE bit is set HIGH (see EDH Flag Detection on page 33).

3.9.8.3 Ancillary Data Checksum Error Correction

When ancillary data checksum error correction and insertion is enabled, the GS9090 will generate and insert ancillary data checksums for all ancillary data words by default. Where user specified ancillary data has been programmed into the ANC_TYPE registers of the host interface (see Programmable Ancillary Data Detection on page 31), only the checksums for the ancillary data programmed will be corrected.

This feature is enabled when the ANC_CSUM_INS bit of the IOPROC_DISABLE register is set LOW.

3.9.8.4 TRS Error Correction

When TRS error correction and insertion is enabled, the GS9090 will generate and insert 10-bit TRS code words as required.

TRS word generation will be performed in accordance with the timing parameters generated by the flywheel to provide an element of noise immunity. As a result, TRS correction will only take place if the flywheel in enabled (FW_EN = HIGH).

In addition, the TRS_INS bit of the IOPROC_DISABLE register must be set LOW.

NOTE: Only H timing based errors will be corrected (see TRS Error Detection on page 43).

3.10 Internal FIFO Operation

The GS9090 contains an internal video line-based FIFO, which can be programmed by the application layer to work in any of the following modes:

1. Video Mode,
2. DVB-ASI Mode,
3. Ancillary Data Extraction Mode, or
4. Bypass Mode

The FIFO can be configured to one of the four modes by using the host interface to set the FIFO_MODE[1:0] bits of the IOPROC_DISABLE register (see Table 3-14 in Error Correction and Insertion on page 43). The setting of these bits is shown in Table 3-15. To enable the FIFO, the application layer must also set the FIFO_EN pin HIGH. Additionally, if the FIFO is configured for video mode or ancillary data extraction mode, the IOPROC_EN pin must be set HIGH.

The FIFO is fully asynchronous, allowing simultaneous read and write access. It has a depth of 2048 words, which will accommodate 1 full line of SD video for both 525 and 625 standards. The FIFO is 15 bits wide: 10 bits for video data and 5 bits for other signals, such as H, V, F, EDH_DETECT, and ANC_DETECT.

Table 3-15: FIFO Configuration Bit Settings

FIFO Mode	FIFO_MODE[1:0] Register Setting	FIFO_EN Pin Setting	IOPROC_EN Pin Setting
Video Mode	00b	HIGH	HIGH
DVB-ASI Mode	01b	HIGH	X
Ancillary Data Extraction Mode	10b	HIGH	HIGH
Bypass Mode	11b	X	X

NOTE: ‘X’ signifies ‘don’t care’. The pin is ignored and may be set HIGH or LOW.

3.10.1 Video Mode

The internal FIFO is in video mode when the application layer sets the FIFO_EN and IOPROC_EN pins HIGH, and the FIFO_MODE[1:0] bits in the IOPROC_DISABLE register are configured to 00b. By default, the FIFO_MODE[1:0] bits are set to 00b by the device whenever the $\overline{\text{SMPTE\_BYPASS}}$ pin is set HIGH and the DVB_ASI pin is set LOW (i.e. the device is in SMPTE mode); however, the application layer may program the FIFO_MODE[1:0] bits as required.

Figure 3-6 shows the input and output signals of the FIFO when it is configured for video mode.

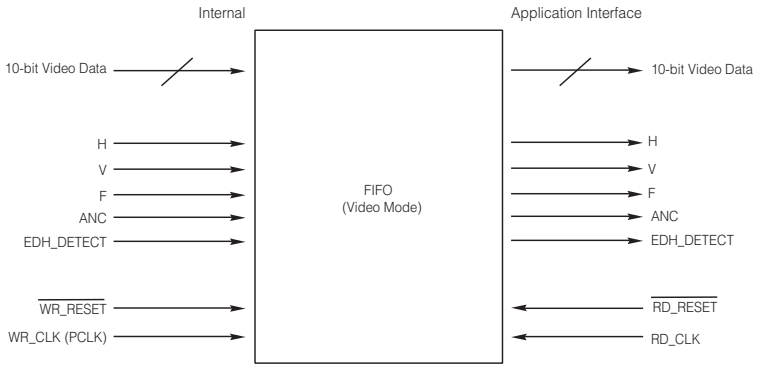


Figure 3-6: FIFO in Video Mode

When operating in video mode, the GS9090 will write data sequentially into the FIFO, starting with the first active pixel in location zero of the memory. In this mode, it is possible to use the FIFO for clock phase interchange and data alignment / delay. The extracted H, V, and F information will also be written into the FIFO. The H, V, and F outputs will be timed to the video data read from the FIFO by the application interface (see HVF Timing Signal Generation on page 28).

The device will ensure write-side synchronization is maintained, according to the extracted PCLK and flywheel timing information.

Full read-control of the FIFO is made available to the application interface such that data will be clocked out of the FIFO on the rising edge of the externally provided RD_CLK signal. When there is a HIGH-to-LOW transition at the $\overline{\text{RD\_RESET}}$ pin the first pixel presented to the video data bus will be the first 000 of the SAV (see Figure 3-7). The $\overline{\text{FIFO\_LD}}$ pulse may be used to control the $\overline{\text{RD\_RESET}}$ pin.

NOTE: The $\overline{\text{RD\_RESET}}$ pulse should not be held LOW for more than one RD_CLK cycle.

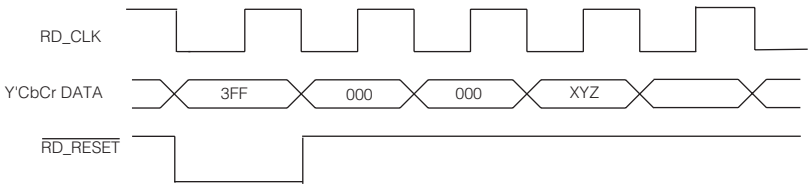


Figure 3-7: $\overline{\text{RD\_RESET}}$ Pulse Timing

In video mode, the ANC_DETECT output signal will be timed to the data output from the FIFO (see Ancillary Data Detection and Indication on page 31 for more detail).

3.10.2 DVB-ASI Mode

The internal FIFO is in DVB-ASI mode when the application layer sets the FIFO_EN pin HIGH, and the FIFO_MODE[1:0] bits in the IOPROC_DISABLE register are configured to 01b. By default, the FIFO_MODE[1:0] bits are set to 01b by the device whenever the DVB_ASI pin is set HIGH (i.e. the device is in DVB-ASI mode); however, the application layer may program the FIFO_MODE[1:0] bits as required.

Figure 3-8 shows the input and output signals of the FIFO when it is configured for DVB-ASI Mode.

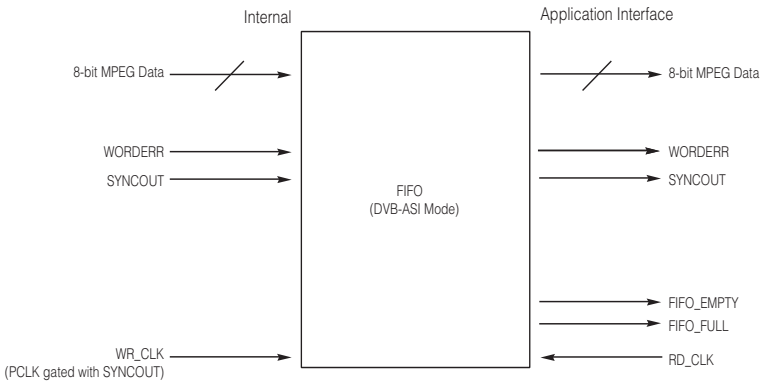


Figure 3-8: FIFO in DVB-ASI Mode

When operating in DVB-ASI mode, the GS9090's FIFO can be used for clock rate interchange operation. The extracted 8-bit MPEG packets will be written into the FIFO at 27MHz based on the SYNCOUT signal from the internal DVB-ASI decoder block. The SYNCOUT and WORDERR bits are also stored in the FIFO (see Status Signal Outputs on page 29).

When SYNCOUT goes HIGH, K28.5 stuffing characters have been detected and no data will be written into the FIFO.

Data is read out of the FIFO by the application layer using the RD_CLK pin. In DVB-ASI mode, the $\overline{\text{RD\_RESET}}$ pin is not used.

3.10.2.1 Reading From the FIFO

The FIFO contains internal read and write pointers used to designate which spot in the FIFO the MPEG packet will be read from or written to. These internal pointers control the status flags FIFO_EMPTY and FIFO_FULL, which are available for output on the multi-function output port pins, if so programmed (see Programmable Multi-Function Outputs on page 56).

In the case where the write pointer is originally ahead of the read pointer, the FIFO_EMPTY flag will be set HIGH when both pointers arrive at the same address (see block A in Figure 3-11). The application layer can use this flag to determine when to stop reading from the device.

A write and read pointer offset may be programmed in the FIFO_EMPTY_OFFSET[9:0] register of the host interface. If an offset value is programmed in this register, the FIFO_EMPTY flag will be set HIGH when the read and write pointers of the FIFO are at the same address, and will remain HIGH until the write pointer reaches the programmed offset. Once the pointer offset has been exceeded, the FIFO_EMPTY flag will go LOW (see block B in Figure 3-11).

In the case where the read pointer is originally ahead of the write pointer, the FIFO_FULL flag will be set HIGH when both pointers arrive at the same address (see block C in Figure 3-11). The application layer can use this flag to determine when to begin reading from the device.

A read and write pointer offset may also be programmed in the FIFO_FULL_OFFSET[9:0] register of the host interface. If an offset value is programmed in this register, the FIFO_FULL flag will be set HIGH when the read and write pointers of the FIFO are at the same address, and will remain set HIGH until the read pointer reaches the programmed offset. Once the pointer offset has been exceeded, the FIFO_FULL flag will be cleared (see block D in Figure 3-11).

Gating the RD_CLK Using the FIFO_EMPTY Flag

Using the asynchronous FIFO_EMPTY flag to gate RD_CLK requires external clock gating circuity to generate a clean burst clock (see Figure 3-9). An example circuit for this application is shown in Figure 3-10.

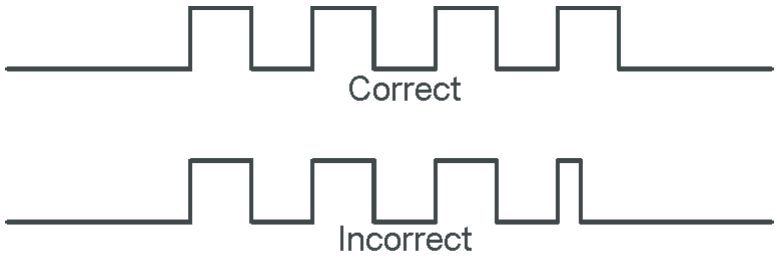


Figure 3-9: Burst Clock

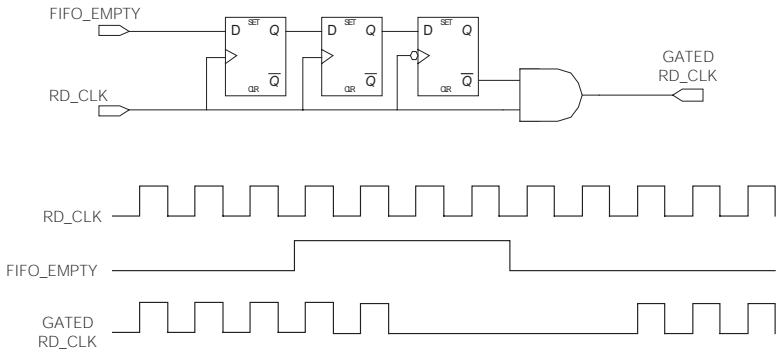


Figure 3-10: Example Circuit to Gate RD_CLK Using the FIFO_EMPTY Flag

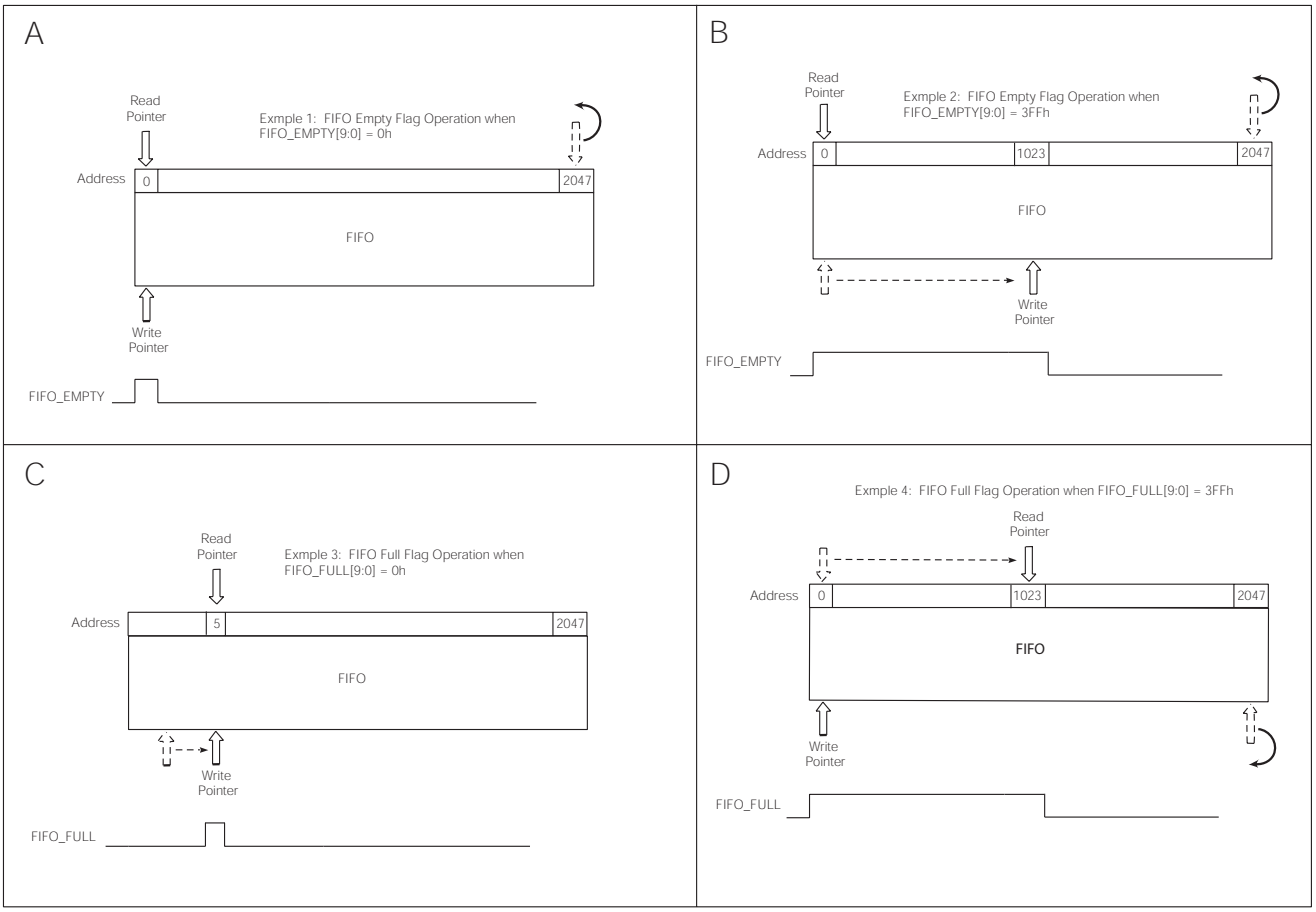


Figure 3-11: Reading From the FIFO in DVB-ASI Mode

3.10.3 Ancillary Data Extraction Mode

The internal FIFO is ancillary data extraction mode when the application layer sets the FIFO_EN and IOPROC_EN pins HIGH, and the FIFO_MODE[1:0] bits in the IOPROC_DISABLE register are configured to 10b.

Once the FIFO enters ancillary data extraction mode, it takes 2200 PCLKs (82us) to initialize the FIFO before ancillary data extraction can begin.

In this mode, the FIFO is divided into two separate blocks of 1024 words each. This allows ancillary data to be written to one side of the FIFO while the application layer reads from the other. Thus, in each half of the FIFO, the GS9090 will write the contents of the packets up to a maximum of 1024 8-bit words.

As described in Programmable Ancillary Data Detection on page 31, up to five specific types of ancillary data to be extracted can be programmed in the ANC_TYPE registers. If the ANC_TYPE registers are all set to zero, the device will extract all types of ancillary data.

The entire packet, including the ancillary data flag (ADF), data identification (DID), secondary data identification (SDID), data count (DC), and checksum word will be written into the memory. The device will detect ancillary data packet DID's placed anywhere in the video data stream, including the active picture area.

Additionally, the lines from which the packets are to be extracted from can be programmed into the ANC_LINE_A[10:0] and ANC_LINE_B[10:0] registers, allowing ancillary data from a maximum of two lines per frame to be extracted. If only one line number register is programmed (with the other set to zero), ancillary data packets will be extracted from one line per frame only. When both registers are set to zero, the device will extract packets from all lines.

The application layer reads the extracted ancillary data through the host interface starting at address 02Ch up to 42Bh inclusive (1024 words). This must be done while there is a valid video signal present at the serial input and the device is locked (LOCKED = HIGH).

3.10.3.1 Ancillary Data Extraction and Reading

To start ancillary data extraction, the ANC_PKT_EXT bit of the IOPROC_DISABLE register must be set HIGH (see Table 3-14 in Error Correction and Insertion on page 43). Packet extraction will begin in the following frame after this bit has been set HIGH.

NOTE: Ancillary data extraction will not begin until 2200 PCLKs (82us) after the device has entered into ancillary data extraction mode (FIFO_MODE[1:0] = 10b), regardless of the setting of the ANC_PKT_EXT bit.

When the FIFO is configured for ancillary data extraction mode, setting the IOPROC_EN pin LOW will disable packet extraction. If IOPROC_EN is LOW, the setting of the ANC_PKT_EXT host interface bit will be ignored.

Clearing the ANC_PKT_EXT bit will not automatically disable ancillary data extraction. To disable ancillary data extraction, switch the FIFO into bypass mode by setting FIFO_MODE[1:0] = 11b. 2200 PCLK cycles after the device re-enters ancillary data extraction mode, data extraction will commence immediately if ANC_PKT_EXT is still HIGH.

The application layer can use the ANC_DETECT output flag available on the I/O output pin (see Programmable Multi-Function Outputs on page 56) to determine the length of the ancillary data extracted and when to begin reading the extracted data from memory. Recall that ANC_DETECT is HIGH whenever ancillary data has been detected.

In addition, the data count (DC) word, which is located three words after the ancillary data flag (ADF) in the memory, can be read to determine how many valid user data words (UDW) are present in the extracted packet (see SMPTE 291M for more details). The DC value can then be used to preset how many address reads must be performed to obtain only the user data words.

Ancillary data will be written into the first half of the FIFO until it is full or until the ANC_DATA_SWITCH bit is toggled (i.e. a HIGH-to-LOW or LOW-to-HIGH transition). If the ANC_DATA_SWITCH bit is not toggled, extracted data will not be written into memory after the first half of the FIFO is full (see block A in Figure 3-12).

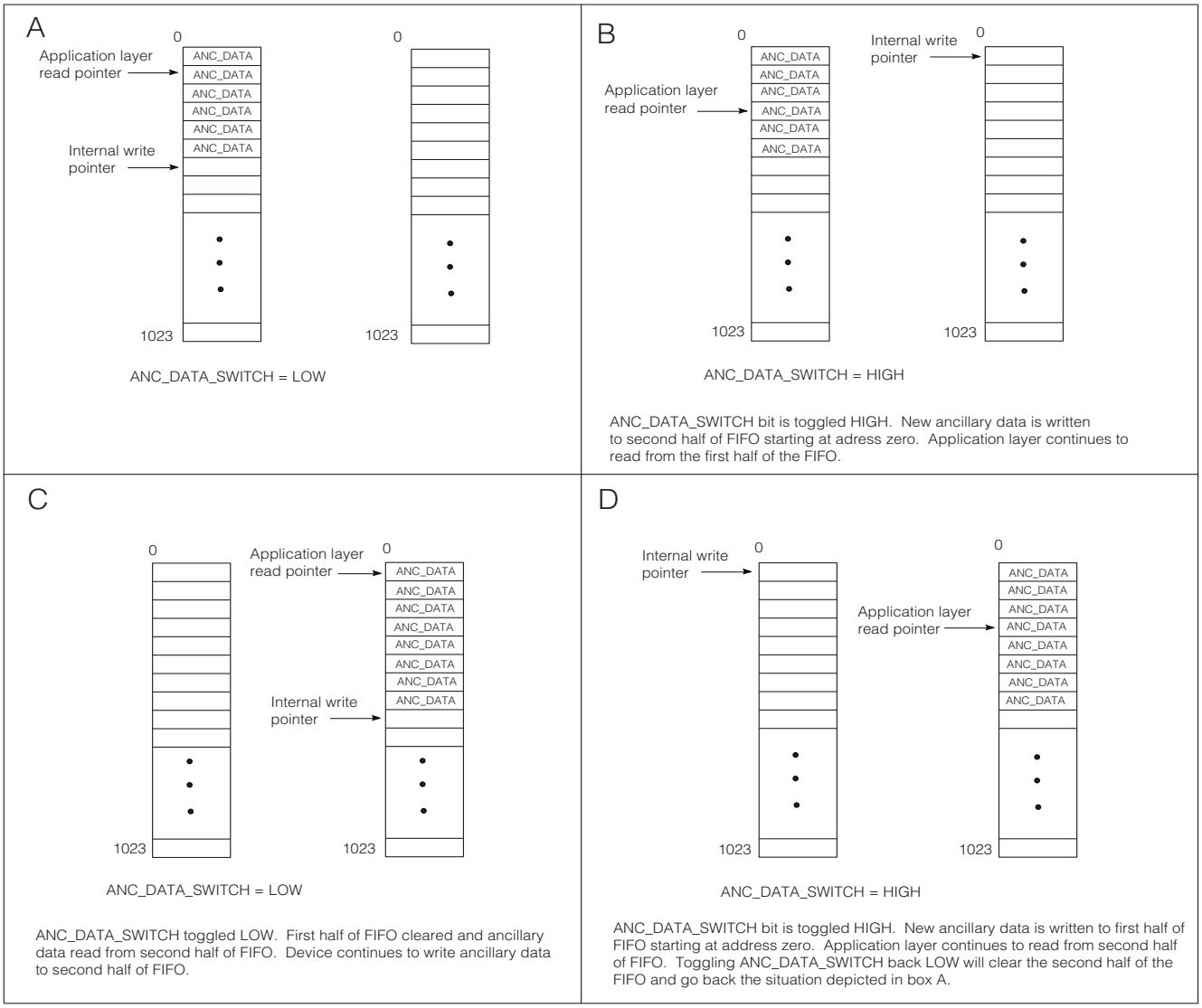
When the ANC_DATA_SWITCH bit is toggled, new extracted data will be written to the second half starting at address zero (see block B in Figure 3-12). The data in the first half of the FIFO may still be read.

Once the data in the first half of the FIFO has been read, the ANC_DATA_SWITCH may be toggled again to enable the second half of the FIFO to be read. The first half of the FIFO will be cleared, and the device will continue to write ancillary data to the second half of the FIFO (see block C in Figure 3-12).

If the ANC_DATA_SWITCH bit is toggled again, new extracted data will be written to the first half starting at address zero (see block D in Figure 3-12). The data in the second half of the FIFO may still be read.

Toggling ANC_DATA_SWITCH again will clear the second half of the FIFO and restore the read and write pointers to the situation shown in block A. The switching process (shown in blocks A to D in Figure 3-12) will continue with each toggle of the ANC_DATA_SWITCH bit.

NOTE: At least 1100 PCLK cycles (41us) must pass between toggles of the ANC_DATA_SWITCH bit. The ANC_DATA_SWITCH bit must be toggled at a point in the video where no extraction is occurring (i.e. the ANC_DETECT signal is LOW).


A
0
Application layer read pointer
ANC_DATA
Internal write pointer
1023
ANC_DATA_SWITCH = LOW
B
Internal write pointer
ANC_DATA_SWITCH = HIGH
ANC_DATA_SWITCH bit is toggled HIGH. New ancillary data is written to second half of FIFO starting at adress zero. Application layer continues to read from the first half of the FIFO.
C
ANC_DATA_SWITCH = LOW
ANC_DATA_SWITCH toggled LOW. First half of FIFO cleared and ancillary data read from second half of FIFO. Device continues to write ancillary data to second half of FIFO.
D
ANC_DATA_SWITCH = HIGH
ANC_DATA_SWITCH bit is toggled HIGH. New ancillary data is written to first half of FIFO starting at address zero. Application layer continues to read from second half of FIFO. Toggling ANC_DATA_SWITCH back LOW will clear the second half of the FIFO and go back the situation depicted in box A.

NOTE: At least 1100 PCLK cycles must pass between toggles of the ANC_DATA_SWITCH bit.
The bit must be toggled at a point where no extraction is occuring (i.e. the ANC signal is LOW).

Figure 3-12: Ancillary Data Extraction and Reading

3.10.3.2 Clearing the ANC Data FIFO

When switching to ANC FIFO mode from any other mode and on power up, the user must follow one of the 2 methods below to ensure that the FIFO is fully cleared.

Clearing ANC FIFO Method 1:

1. Enable ANC FIFO mode (write 10b into the FIFO_MODE register).
2. Wait for ANC_FIFO_READY bit to be asserted.
3. Toggle (LOW-to-HIGH-to-LOW) ANC_DATA_SWITCH bit (bit 12 of IO_CONFIG register) twice.

Clearing ANC FIFO Method 2:

1. Power on device.
2. Set FIFO_EN pin HIGH.
3. Enable ANC FIFO mode (write 10b into the FIFO_MODE register).
4. Set FIFO_EN pin LOW.
5. Set FIFO_EN pin HIGH.

3.10.4 Bypass Mode

The internal FIFO is in bypass mode when the application layer sets the FIFO_EN or IOPROC_EN pin LOW, or the FIFO_MODE[1:0] bits in the IOPROC_DISABLE register are configured to 11b. By default, the FIFO_MODE[1:0] bits are set to 11b by the device whenever both the SMPTE_BYPASS and DVB_ASI pins are LOW; however, the application layer may program the FIFO_MODE[1:0] bits as required.

In bypass mode, the FIFO is not inserted into the video path and data is presented to the output of the device synchronously with the PCLK output. The FIFO will be disabled and placed in static mode to save power.

3.11 Parallel Data Outputs

Data outputs are valid on the rising edge of PCLK as shown in Figure 3-13.

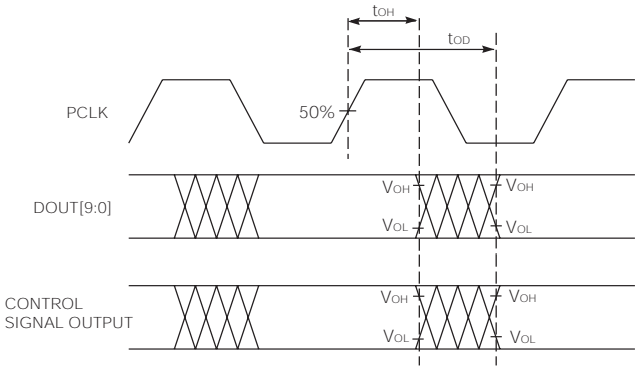


Figure 3-13: PCLK to Data & Control Signal Output Timing

The data is presented in 10-bit format and may be scrambled or unscrambled, framed or unframed.

The output data format is defined by the settings of the external $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins (see Table 3-16). Recall that in Manual mode, these pins are set by the application layer as inputs to the device. In Auto mode, however, the GS9090 sets these pins as output status signals.

Table 3-16: Parallel Data Output Format

		Pin Settings	
Output Data Format	**DOUT[9:0]**	**$\overline{\text{SMPTE\_BYPASS}}$**	**DVB_ASI**
10-bit Data	DATA	LOW	LOW
10-bit Multiplexed SD	Luma / Chroma	HIGH	LOW
10-bit DVB-ASI	DVB-ASI data	LOW	HIGH

3.11.1 Parallel Data Bus

The parallel data outputs of the GS9090 support both LVTTL and LVCMOS levels. These outputs use either +1.8V or +3.3V, supplied at the IO_VDD and IO_GND pins. When interfacing with +5V logic levels, the IO_VDD pins should be supplied with +3.3V. For a low power connection, the IO_VDD pins may be connected to +1.8V.

All outputs, including the PCLK output, will be driven to a high-impedance state if the $\overline{\text{RESET}}$ signal is asserted LOW with the exception of the STAT pins and the $\overline{\text{DATA\_ERROR}}$ pin which will maintain the last state they were in for the duration that $\overline{\text{RESET}}$ is asserted.

3.11.2 Parallel Output in SMPTE Mode

When the device is operating in SMPTE mode (see SMPTE Functionality on page 25), SD data is presented to the output bus in multiplexed format. The data will be output on the DOUT[9:0] pins and word aligned according to TRS ID words.

3.11.3 Parallel Output in DVB-ASI Mode

When operating in DVB-ASI mode (see DVB-ASI Functionality on page 29), the extracted 8-bit data words will be presented on DOUT[7:0] such that DOUT7 = HOUT is the most significant bit of the decoded transport stream data and DOUT0 = AOUT is the least significant bit.

In addition, DOUT9 and DOUT8 will be configured as the DVB-ASI status signals WORDERR and SYNCOUT respectively. See Status Signal Outputs on page 29 for a description of these DVB-ASI specific output signals.

3.11.4 Parallel Output in Data-Through Mode

When operating in Data-Through mode (see Data-Through functionality on page 29), the GS9090 presents data to the output data bus without performing any decoding, descrambling, or word-alignment.

As described in Data-Through functionality on page 29, the data bus outputs will be forced to logic LOW if the device is set to operate in Auto mode but cannot identify SMPTE TRS ID or DVB-ASI sync words in the input data stream.

3.12 Programmable Multi-Function Outputs

The GS9090 has a multi-function output port that uses 4 pins, STAT0 through STAT3. Each pin can be programmed via the host interface to output one of the following signals: H, V, F, $\overline{\text{FIFO\_LD}}$, ANC_DETECT, EDH_DETECT, FIFO_FULL, and FIFO_EMPTY.

Table 3-17: Output Signals Available on Multi-Function Output Ports

Output Status Signal	Reference
H	HVF Timing Signal Generation on page 28
V	HVF Timing Signal Generation on page 28
F	HVF Timing Signal Generation on page 28
$\overline{\text{FIFO\_LD}}$	FIFO Load Pulse on page 30
ANC_DETECT	Ancillary Data Detection and Indication on page 31
EDH_DETECT	EDH Packet Detection on page 33
FIFO_FULL	Reading From the FIFO on page 48
FIFO_EMPTY	Reading From the FIFO on page 48

The registers that determine the signals present on the STAT [3:0] pins are labelled STAT0_CONFIG[2:0], STAT1_CONFIG[2:0], STAT2_CONFIG[2:0], and STAT3_CONFIG[2:0] respectively. Table 3-18 shows the setting of the IO_CONFIG registers for each of the available output signals.

Table 3-18: IO_CONFIG Settings

Function	I/O	IO_CONFIG Setting
H	Output	000b
V	Output	001b
F	Output	010b
$\overline{\text{FIFO\_LD}}$	Output	011b
ANC_DETECT	Output	100b
EDH_DETECT	Output	101b
FIFO_FULL	Output	110b
FIFO_EMPTY	Output	111b

The default setting for each IO_CONFIG register depends on the configuration of the device and the internal FIFO mode selected. This is shown in Table 3-19.

NOTE: Signals not relevant to the particular mode of operation will be ignored and be high-impedance when programmed to be displayed on the STAT[3:0] pins. For example, the FIFO_FULL and FIFO_EMPTY flags can only be displayed on the STAT[3:0] pins when the device is in DVB-ASI mode. If the FIFO_FULL or FIFO_EMPTY value (110 and 111 respectively) is programmed into the IO_CONFIG registers when the device is in SMPTE mode, the value will be ignored and the I/O pin will be set to a high impedance state.

Table 3-19: STAT [3:0] Output Default Configuration

Device Configuration	IO_CONFIG Register	I/O	Function	Default IO_CONFIG Setting
SMPTE Functionality $\overline{\text{SMPTE\_BYPASS}}$ = HIGH DVB_ASI = LOW FIFO: Video Mode or Ancillary Data Extraction Mode	STAT0_CONFIG	Output	H	000b
	STAT1_CONFIG	Output	V	001b
	STAT2_CONFIG	Output	F	010b
	STAT3_CONFIG	Output	$\overline{\text{FIFO\_LD}}$	011b
DVB-ASI DVB_ASI = HIGH FIFO: DVB-ASI Mode	STAT0_CONFIG	Output	FIFO_FULL	110b
	STAT1_CONFIG	Output	FIFO_EMPTY	111b
	STAT2_CONFIG	Output	High Z	000b
	STAT3_CONFIG	Output	High Z	000b

Table 3-19: STAT [3:0] Output Default Configuration (Continued)

Device Configuration	IO_CONFIG Register	I/O	Function	Default IO_CONFIG Setting
Data-Through SMPTE_BYPASS = LOW DVB_ASI = LOW	STAT0_CONFIG	Output	High Z	000b
	STAT1_CONFIG	Output	High Z	000b
	STAT2_CONFIG	Output	High Z	000b
	STAT3_CONFIG	Output	High Z	000b

3.13 GS9090 Low-latency Mode

When the IOPROC_EN pin is set LOW, the GS9090 will enter a low-latency mode such that the parallel data will be output with the minimum PCLK latency possible. The FIFO and all processing blocks except the descrambling and word alignment blocks will be bypassed when $\overline{\text{SMPTE\_BYPASS}}$ is HIGH.

Low-latency mode will also be selected when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW, regardless of the setting of the IOPROC_EN signal (see Table 3-20).

In DVB-ASI mode, the device will have a higher latency than low-latency mode, although this latency will be less than SMPTE mode.

NOTE: When in low-latency mode, the STAT pin output of the ANC packet flag is delayed by 15 PCLK cycles with respect to the parallel video output. The length of the flag matches the length of the ANC packet.

Table 3-20: Pin Settings in Low-latency Mode

IOPROC_EN Setting	$\overline{\text{SMPTE\_BYPASS}}$ Setting	Latency (PCLK Cycles)
LOW	LOW	9
HIGH	LOW	10
LOW	HIGH	10
HIGH	HIGH	25

NOTE: Latency applies to parallel processing core only.

When the GS9090 is configured for low-latency mode, the H, V, and F output timing will be TRS based blanking only as shown in Figure 3-14. Active line-based timing is not available and the setting of the H_CONFIG host interface bit will be ignored.

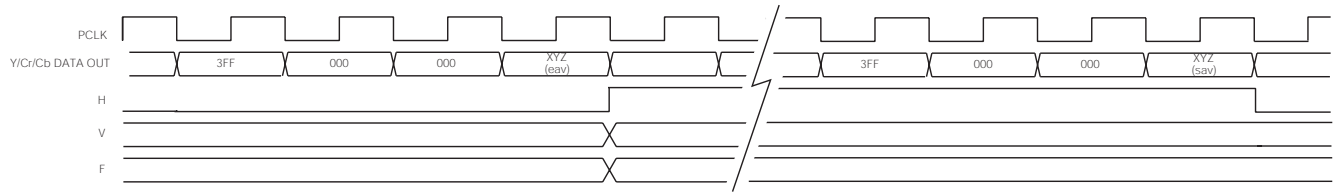


Figure 3-14: H,V,F Timing In Low-latency Mode

3.14 GSPI Host Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the host to enable additional features of the GS9090 and/or to provide additional status information through configuration registers in the device.

The GSPI comprises a serial data input signal SDIN, serial data output signal SDOUT, an active low chip select $\overline{CS}$, and a burst clock SCLK.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the application interface. The SDOUT pin is a non-clocked loop-through of SDIN and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. The interface is illustrated in Figure 3-15.

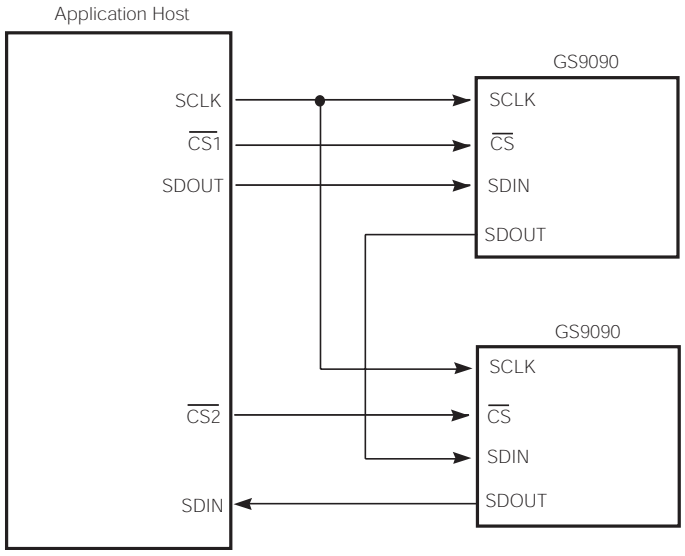


Figure 3-15: GSPI Application Interface Connection

All read or write access to the GS9090 is initiated and terminated by the host processor. Each access always begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

3.14.1 Command Word Description

The command word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address. Figure 3-16 shows the command word format and bit configurations.

Command words are clocked into the GS9090 on the rising edge of the serial clock SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each command word must be followed by only one data word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following data word will be written into the address specified in the command word, and subsequent data words will be written into incremental addresses from the previous data word. This facilitates multiple address writes without sending a command word for each data word.

Auto-Increment may be used for both read and write access.

3.14.2 Data Read and Write Timing

Read and write mode timing for the GSPI interface is shown in Figure 3-18 and Figure 3-19 respectively. The timing parameters are defined in Table 3-21.

When several devices are connected to the GSPI chain, only one $\overline{CS}$ must be asserted during a read sequence.

During the write sequence, all command and following data words input at the SDIN pin are output at the SDOUT pin as is. Where several devices are connected to the GSPI chain, data can be written simultaneously to all the devices that have $\overline{CS}$ set LOW.

Table 3-21: GSPI Timing Parameters

Parameter	Definition	Specification
t_0	The minimum duration of time chip select, $\overline{CS}$, must be LOW before the first SCLK rising edge.	1.5 ns
t_1	The minimum SCLK period.	18.5 ns
t_2	Duty cycle tolerated by SCLK.	40% to 60%
t_3	Minimum input setup time.	1.5 ns
t_4	Write Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	37.1 ns
t_5	Read Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	148.4 ns
t_5	Read Cycle - FIFO in ANC Extraction Mode: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	222.6 ns
t_6	Minimum output hold time.	1.5 ns

Table 3-21: GSPI Timing Parameters (Continued)

Parameter	Definition	Specification
t_7	The minimum duration of time between the last SCLK of the GSPI transaction and when $\overline{CS}$ can be set HIGH.	37.1 ns
t_8	Minimum input hold time.	1.5 ns

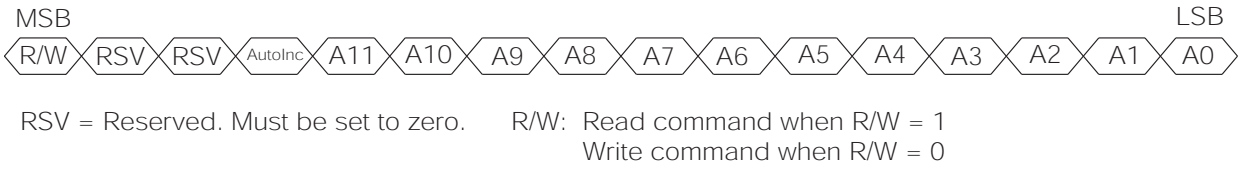


Figure 3-16: Command Word Format

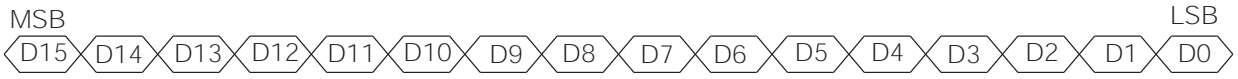


Figure 3-17: Data Word Format

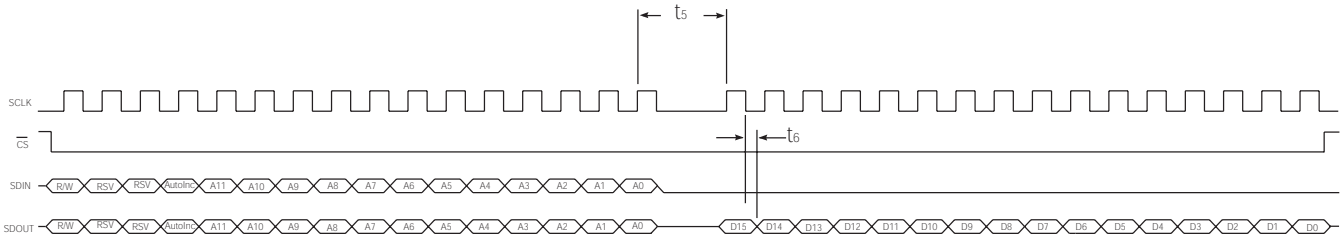


Figure 3-18: GSPI Read Mode Timing

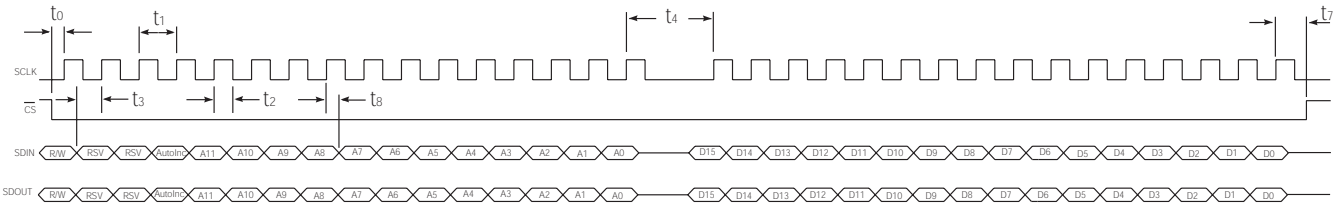


Figure 3-19: GSPI Write Mode Timing

3.14.3 Configuration and Status Registers

Table 3-22 summarizes the GS9090's internal status and configuration registers.

All of these registers are available to the host via the GSPI and are all individually addressable.

Where status registers contain less than the full 16 bits of information, two or more registers may be combined at a single logical address.

Table 3-22: GS9090 Internal Registers

Address	Register Name	Reference
00h	IOPROC_DISABLE	Error Correction and Insertion on page 43
01h	ERROR_STATUS	Error Detection and Indication on page 38
02h	EDH_FLAG_IN	EDH Flag Detection on page 33
03h	EDH_FLAG_OUT	EDH Flag Detection on page 33
04h	DATA_FORMAT	Video Standard Indication on page 38
05h	IO_CONFIG	Programmable Multi-Function Outputs on page 56
06h	FIFO_EMPTY_OFFSET	Reading From the FIFO on page 48
07h	FIFO_FULL_OFFSET	Reading From the FIFO on page 48
08h - 0Eh	ANC_TYPE	Ancillary Data Detection and Indication on page 31
11h - 14h	RASTER_STRUCTURE	Automatic Video Standard and Data Format Detection on page 37
15h - 24h	EDH_CALC_RANGES	EDH CRC Error Detection on page 40
25h	ERROR_MASK	Error Detection and Indication on page 38
28h	FIFO_LD_POSITION	Programmable FIFO Load Position on page 30
02Ch - 42Bh	INTERNAL FIFO	Ancillary Data Extraction Mode on page 51

3.15 Reset Operation

When the $\overline{\text{RESET}}$ signal on the GS9090 is de-asserted ($\overline{\text{RESET}}$ = LOW to HIGH) the LOCKED and DATA[9:0] signals are valid after a period of 200ns after fhe rising edge of the $\overline{\text{RESET}}$ signal. (See Figure 3-20)

The application layer should not sample the LOCKED or DATA[9:0] signals during this time.

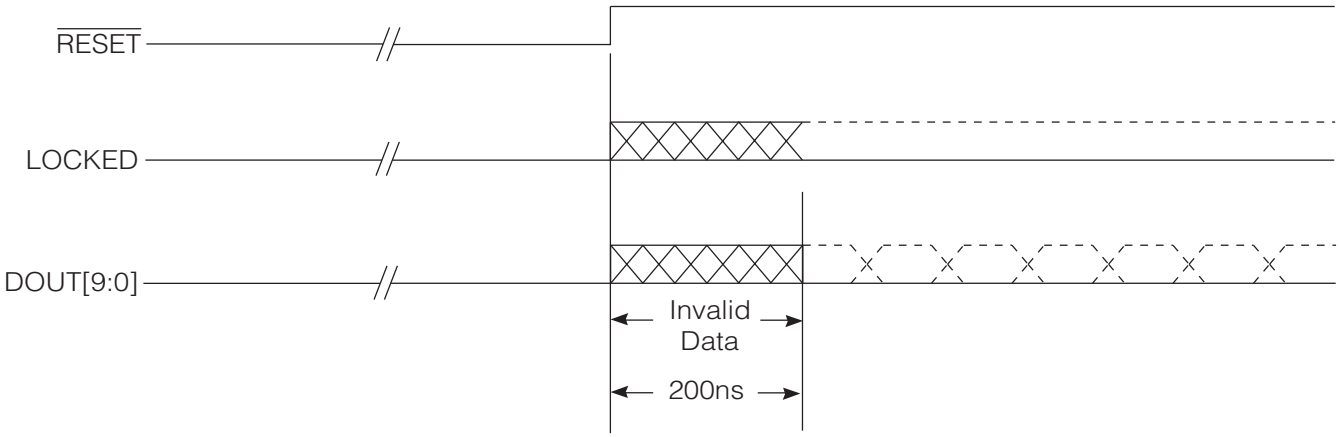


Figure 3-20: Reset Timing

3.16 JTAG Operation

When the JTAG/$\overline{\text{HOST}}$ pin is set HIGH by the application layer, the host interface port (as described in GSPI Host Interface on page 59) will be configured for JTAG test operation. In this mode, pins 16, 17, 19, and 20 become TMS, TCK, TDO, and TDI respectively. In addition, the $\overline{\text{RESET}}$ pin will operate as the test reset pin, as well as resetting the internal registers.

Boundary scan testing using the JTAG interface will be possible in this mode.

There are two methods in which JTAG can be used on the GS9090:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly; or
2. Under control of the host for applications such as system power self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ input signal. This is shown in Figure 3-21.

Alternatively, if the test capabilities are to be used in the system, the host may still control the JTAG/$\overline{\text{HOST}}$ input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 3-22.

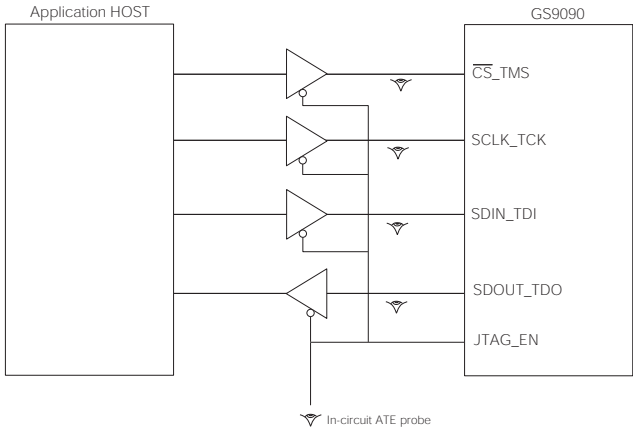


Figure 3-21: In-Circuit JTAG

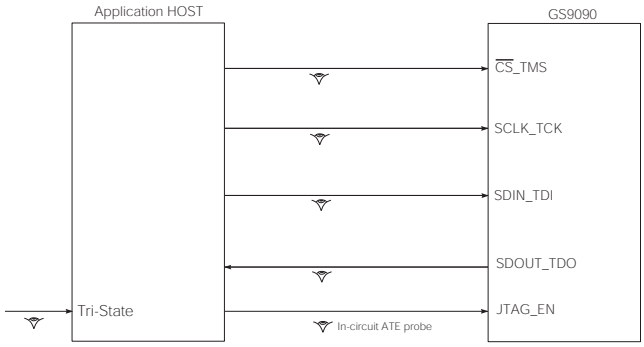


Figure 3-22: System JTAG

3.17 Device Power Up

The GS9090 has a recommended power supply sequence. To ensure correct power up, power the CORE_VDD pins before the IO_VDD pins. In order to initialize all internal operating conditions to their default state the application layer must hold the RESET pin LOW for a minimum of t_{reset} = 1ms. (See Figure 3-23)

Device pins can be driven prior to power up without causing damage.

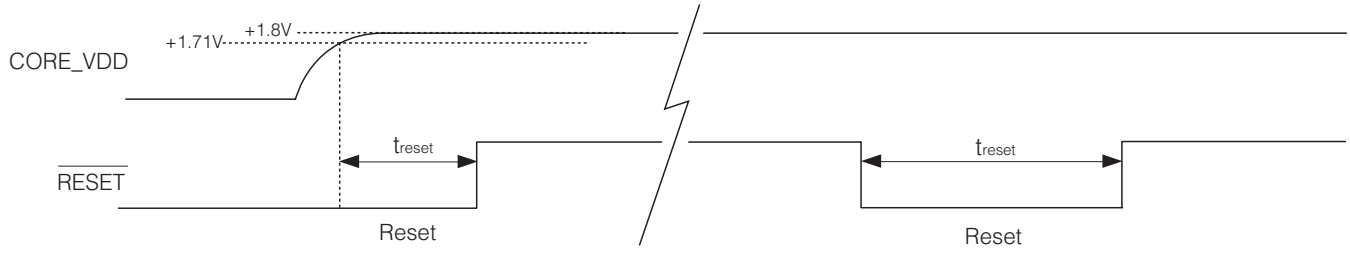


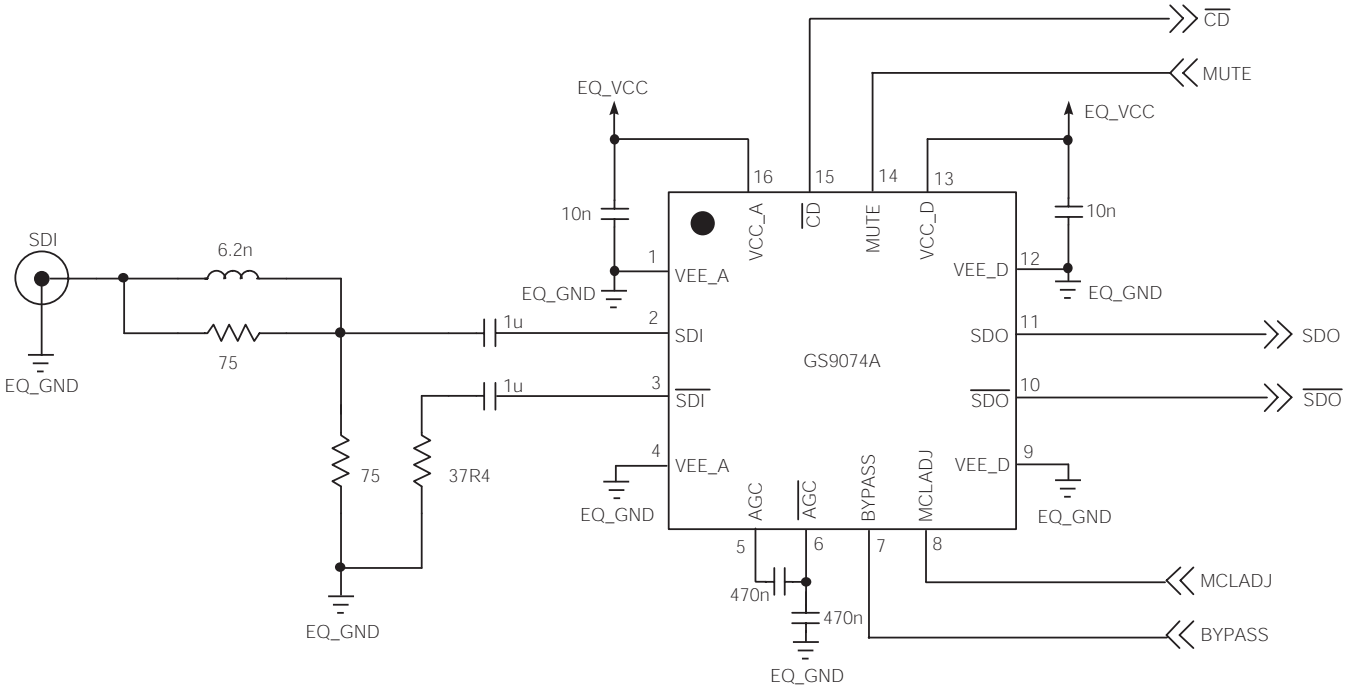
Figure 3-23: Reset pulse

4. References & Relevant Standards

SMPTE 125M	Component video signal 4:2:2 – bit parallel interface
SMPTE 259M	10-Bit 4:2:2 Component and $4f_{SC}$ Composite Digital Signals - Serial Digital Interface
SMPTE 291M	Ancillary Data Packet and Space Formatting
SMPTE 293M	720 x 483 active line at 59.94 Hz progressive scan production – digital representation
SMPTE 305.2M	Serial Data Transport Interface
SMPTE 352M	Video Payload Identification for Digital Television Interfaces
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE RP168	Definition of Vertical Interval Switching Point for Synchronous Video Switching

5. Application Information

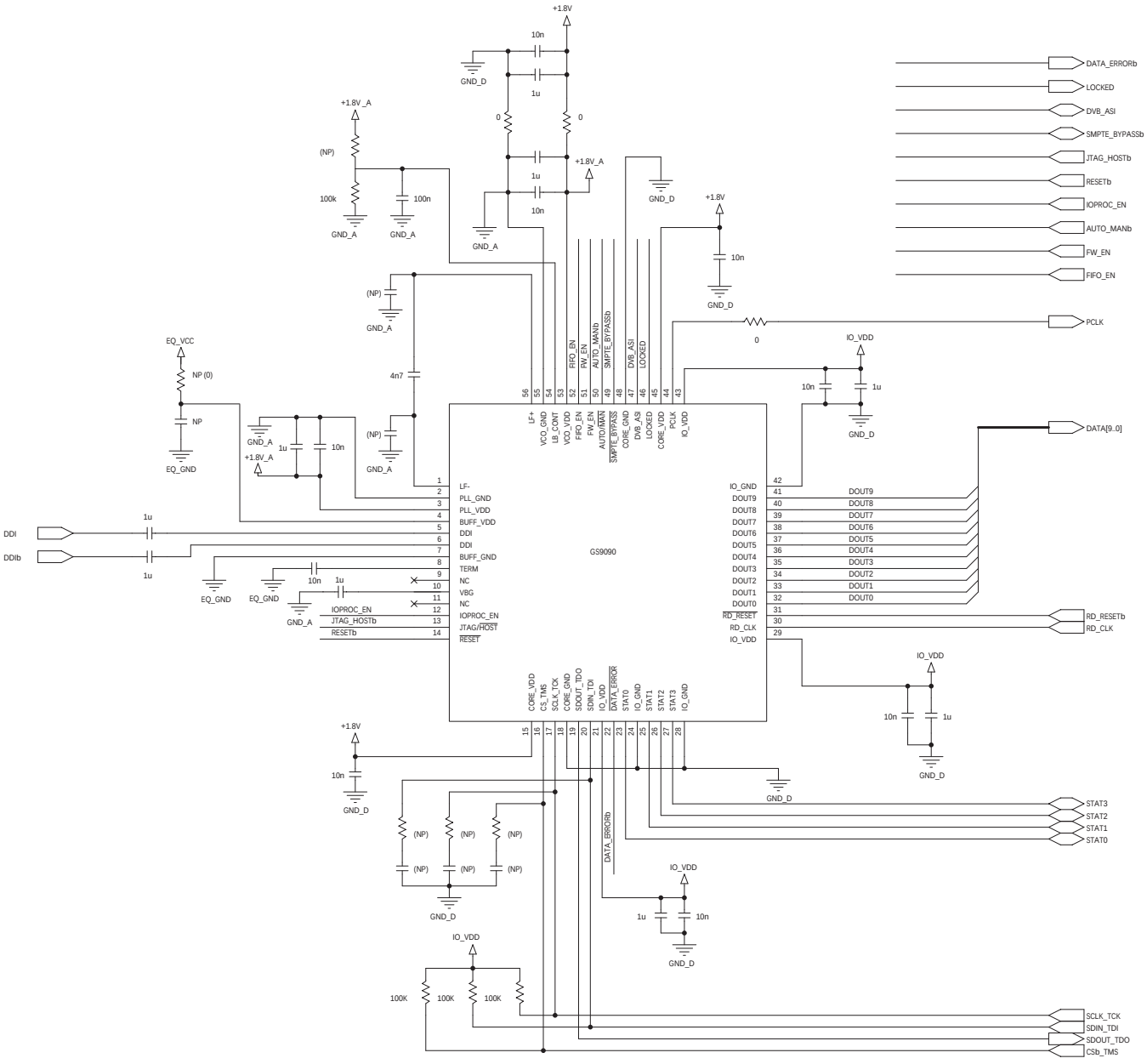
5.1 Typical Application Circuit (Part A)



NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

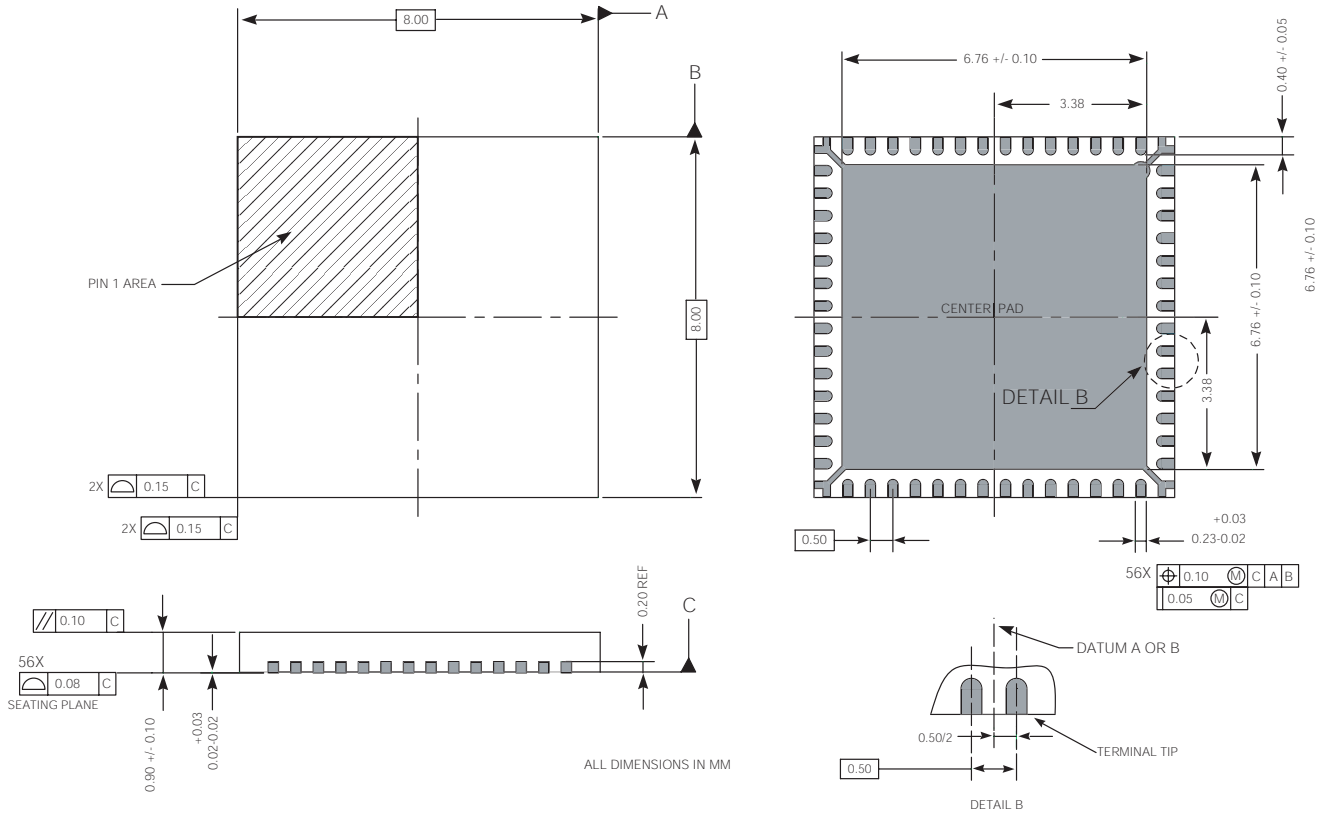
NOTE: For up-to-date component values and detailed operation of the equalizer, please see the GS9074A data sheet.

5.2 Typical Application Circuit (Part B)

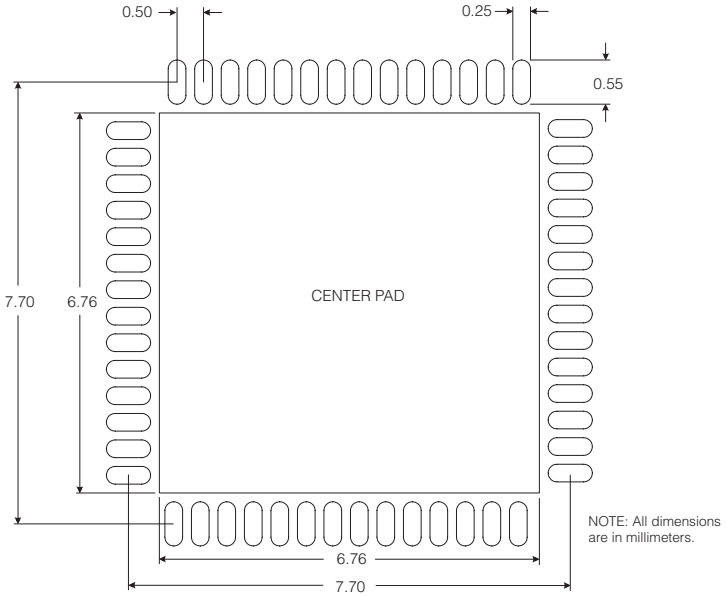


6. Package & Ordering Information

6.1 Package Dimensions



6.2 Recommended PCB Footprint



The Center Pad of the PCB footprint should be connected to the CORE_GND plane by a minimum of 25 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	8mm x 8mm 56-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	12.2°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	25.8°C/W
Psi	9.1°C/W
Pb-free and RoHS compliant	Yes

6.4 Ordering Information

Part Number	Package	Temperature Range
GS9090-CNE3	56-pin QFN	0°C to 70°C

7. Revision History

Version	ECR	Date	Changes and/or Modifications
A	130109	August 2003	New Document.
B	133382	April 2004	Reflected recent design changes in Section 3. Updated Electrical Characteristics tables. Expanded section on EDH flags. Transferred document to new template.
C	133757	June 2004	Modified Section 3.16. Added new reflow profiles.
0	135948	March 2005	Converted to Preliminary Data Sheet. Updated pinout diagram to show center pad. Updated pin descriptions to add center pad. Added Reset Operation section. Updated Package Dimensions to provide clarity on center pad. Added Packaging Data Section. Added Recommended PCB Footprint Section. Updated Absolute Maximum Ratings table. Added Application Information Section with Typical Application Circuits.
1	136665	July 2005	Converted to Data Sheet. Updated input swing minimum value in AC electrical characteristics and added Figure 2-1 to clarify meaning. Updated GSPI SCLK to show as a burst clock rather than a continuous one. Corrected the units for Input Termination Resistance in the DC Electrical Characteristics table. Updated ESD notes in Absolute Maximum Ratings table. Updated Operational Temperature Range in DC Electrical Characteristics table. Corrected minor typing errors.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

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